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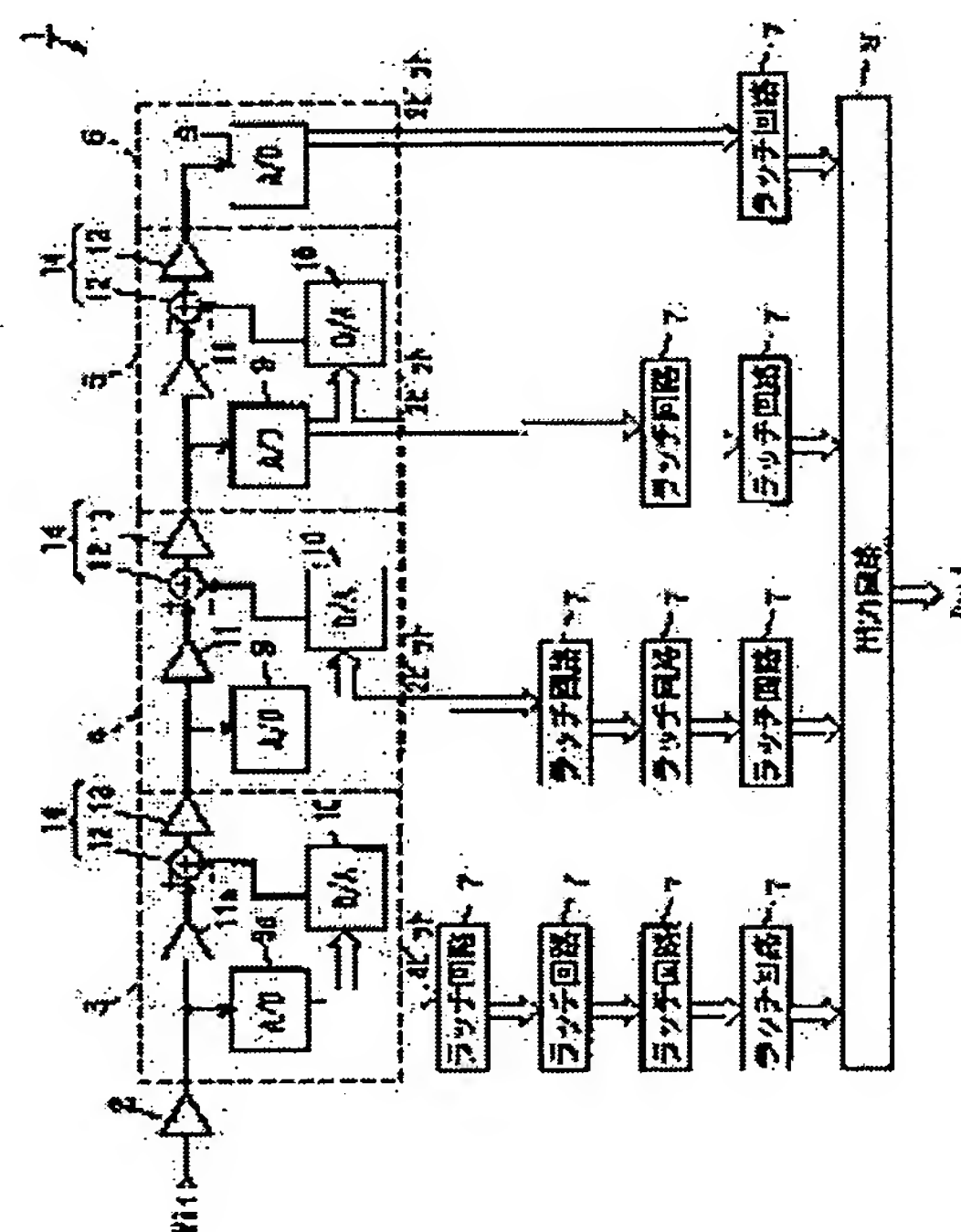
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(54) ANALOG/DIGITAL CONVERTER CIRCUIT

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a pipeline type analog/digital (A/D) converter circuit in which a change in the voltage range of an analog input signal or change of an input system between a differential double end input and a single end input can be easily performed without redesigning a circuit configuration.

SOLUTION: When the voltage range of the analog input signal is V_{INp-p} , the full scale range of a sub A/D converter 9 is switched to V_{INp-p} , and the gain of an operational amplifier circuit 11a is switched into single. When the voltage range of the analog input signal is $V_{INp-p}/2$, the full scale range of the sub A/D converter 9 is switched to $V_{INp-p}/2$ and the gain of the operational amplifier circuit 11a is switched into double.



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* NOTICES *

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2.**** shows the word which can not be translated.

3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]

[Claim 1]An analog-to-digital circuit comprising:

An analog-digital converter which has the multi stage pipeline constitution which consists of two or more steps of circuits and from which a circuit of each stage except a circuit of a final stage changes an inputted analog signal into a digital signal.

A digital-to-analog converter which changes into an analog signal a digital signal outputted from said analog-digital converter.

Have the 1st arithmetic amplifier that amplifies difference of an analog signal inputted and an analog signal outputted from said digital-to-analog converter, and a circuit of a final stage, An analog-digital converter which changes an inputted analog signal into a digital signal is included, An analog-digital converter which has a switching means from which at least one step of circuit except a circuit of a final stage changes a full-scale range to two or more steps, At least one of the 1st arithmetic amplifiers that have a switching means which changes a digital-to-analog converter and a profit which have a switching means which changes a full-scale range to two or more steps to two or more steps is included, And/or, an analog-digital converter which has a switching means from which a circuit of a final stage changes a full-scale range to two or more steps.

[Claim 2]A circuit of each stage except a circuit of a final stage includes further the 2nd arithmetic amplifier that amplifies an inputted analog signal and is given to said 1st arithmetic amplifier, The analog-to-digital circuit according to claim 1, wherein said 2nd arithmetic amplifier of at least one step of circuit except a circuit of a final stage has a switching means which changes a profit to two or more steps.

[Claim 3]The analog-to-digital circuit according to claim 1 or 2, wherein said 1st arithmetic amplifier of at least one step of circuit except a circuit of a final stage has a switching means which changes a profit to two or more steps.

[Claim 4]The analog-to-digital circuit according to any one of claims 1 to 3, wherein said analog-digital converter of at least one step of circuit has a switching means which changes a full-scale range to two or more steps.

[Claim 5]The analog-to-digital circuit according to any one of claims 1 to 4, wherein said digital-to-analog converter of at least one step of circuit except a circuit of a final stage has a switching means which changes a full-scale range to two or more steps.

[Claim 6]Said 2nd arithmetic amplifier of at least one step of said circuit, On a profit which becomes settled with a value of said input capacitance, and a value of said feedback capacity, have input capacitance, feedback capacity, and an operational amplifier, amplify an inputted analog signal, and said switching means, The analog-to-digital circuit according to claim 2 containing a variable region which sets either [at least] a value of said input capacitance, or a value of said feedback capacity as variable.

[Claim 7]The analog-to-digital circuit according to claim 6, wherein said variable region contains a switch part changed to a state or the state where it connected too hastily where a part of said input capacitance or said feedback capacity was separated.

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[Claim 8] Said 1st arithmetic amplifier of at least one step of said circuit, On a profit which becomes settled with a value of said input capacitance, and a value of said feedback capacity, have input capacitance, feedback capacity, and an operational amplifier, amplify an inputted analog signal, and said switching means, The analog-to-digital circuit according to claim 3 containing a variable region which sets either [at least] a value of said input capacitance, or a value of said feedback capacity as variable.

[Claim 9] The analog-to-digital circuit according to claim 8, wherein said variable region contains a switch part changed to a state or the state where it connected too hastily where a part of said input capacitance or said feedback capacity was separated.

[Claim 10] The analog-to-digital circuit according to claim 9 characterized by connecting said switch part to said 2nd capacity in series or in parallel including the 1st and 2nd capacity by which said feedback capacity was provided in parallel or in series between an input terminal of said operational amplifier, and an output terminal.

[Claim 11] The analog-to-digital circuit according to claim 10, wherein said switch part is connected to an output terminal of said operational amplifier.

[Claim 12] The analog-to-digital circuit according to claim 9 characterized by connecting said switch part to said 2nd capacity in series or in parallel including the 1st and 2nd capacity by which said input capacitance was provided in an input terminal of said operational amplifier in parallel or in series.

[Claim 13] The analog-to-digital circuit according to claim 12 connecting to an input side of said 2nd capacity before said switch part.

[Claim 14] The analog-to-digital circuit comprising according to claim 4:

Circuit generating reference voltage where said analog-digital converter of at least one step of circuit generates two or more reference voltage.

A variable region which sets as variable two or more reference voltage in which said switching means is generated by said circuit generating reference voltage including two or more comparators compared with an analog signal into which two or more reference voltage generated by said circuit generating reference voltage was inputted.

[Claim 15] The analog-to-digital circuit comprising according to claim 5:

Circuit generating reference voltage where said digital-to-analog converter of at least one step of circuit except a circuit of a final stage generates reference voltage.

Two or more capacity connected to a common terminal.

Two or more switches which give reference voltage which was connected between said circuit generating reference voltage and said two or more capacity, and was generated by said circuit generating reference voltage according to a digital signal inputted to said two or more capacity, respectively are included, A variable region which sets as variable reference voltage in which said switching means is generated by said circuit generating reference voltage.

[Translation done.]

the full-scale range of sub A/D converter 9] $V_{IN_{p-p}}$ twice many / 4 in order to take consistency with the output voltage range of the arithmetic amplifier 11 which has the profit 2.

[0010]Next, operation of the analog-to-digital circuit 1 of drawing 23 is explained. The sample hold circuit 2 samples the analog input signal V_{in} , and carries out fixed time maintenance. The analog input signal V_{in} outputted from the sample hold circuit 2 is transmitted to the 1st step of circuit 3.

[0011]In the 1st step of circuit 3, sub A/D converter 9 performs an analog to digital to the analog input signal V_{in} of voltage range $V_{IN_{p-p}}$. Here, the full-scale range of sub A/D converter 9 is $V_{IN_{p-p}}$ as mentioned above. The digital output ($2^9, 2^8, 2^7, 2^6$) which is an analog-to-digital result of sub A/D converter 9 is transmitted to the output circuit 8 via the four latch circuitry 7 while it is transmitted to D/A converter 10. The normal output voltage range of D/A converter 10 is expressed like a following formula.

[0012]

(The 1st step of resolution-1) x(full-scale range of D/A converter 10)/(the 1st step of resolution)

$= (2^4 - 1) \times (V_{IN_{p-p}}) / 2^4 = 15V_{IN_{p-p}} / 16$ one side and the arithmetic amplifier 11 sample the analog input signal V_{in} , and amplify and hold it. The output voltage range of the arithmetic amplifier 11 is expressed like a following formula.

[0013]

(Voltage range $V_{IN_{p-p}}$ of the analog input signal V_{in}) x (profit of the arithmetic amplifier 11)

$= \text{The } V_{IN_{p-p}} \times 1 = V_{IN_{p-p}}$ subtraction amplifier 14 subtracts and amplifies the analog input signal V_{in} and the D/A conversion result of D/A converter 10 which were outputted from the arithmetic amplifier 11. The output of the subtraction amplification width circuit 14 is transmitted to the 2nd step of circuit 4. The output voltage range of the 1st step of subtraction amplifier 14 is expressed like a following formula.

[0014]

(Output voltage range of the arithmetic amplifier 11) x (- (normal output voltage range of D/A converter 10)) (profit of the subtraction amplifier 14)

$= (V_{IN_{p-p}}) (- (15V_{IN_{p-p}} / 16))$ In the x2 $= V_{IN_{p-p}} / 82$ step circuit 4, sub A/D converter 9 performs an A/D conversion to the output of the subtraction amplifier 14 of the 1st step of circuit 3. The A/D conversion result of sub A/D converter 9 is transmitted to the output circuit 8 via the three latch circuitry 7 while it is transmitted to D/A converter 10. Thereby, a 2-bit digital output ($2^5, 2^4$) is obtained at least for Nakagami from the 2nd step of circuit 4. The normal output voltage range of D/A converter 10 is expressed like a following formula.

[0015]

(The 2nd step of resolution-1) x(full-scale range of D/A converter 10)/(the 2nd step of resolution)

$= (2^2 - 1) \times (V_{IN_{p-p}} / 4) / 2^2 = 3V_{IN_{p-p}} / 16$ one side and the arithmetic amplifier 11 amplify the output of the arithmetic amplifier 13 of the 1st step of circuit 3. The output voltage range of the arithmetic amplifier 11 is expressed like a following formula.

[0016]

(Output voltage range of the 1st step of subtraction amplifier 14) x (profit of the arithmetic amplifier 11)

$= (V_{IN_{p-p}} / 8)$ The x2 $= V_{IN_{p-p}} / 4$ subtraction amplifier 14 subtracts and amplifies the output of the arithmetic amplifier 11, and the D/A conversion result of D/A converter 10. The output of the subtraction amplifier 14 is transmitted to the 3rd step of circuit 5. The range of the output voltage of the 2nd step of subtraction amplifier 14 is expressed like a following formula.

[0017]

(Output voltage range of the arithmetic amplifier 11) x (- (normal output voltage range of D/A converter 10)) (profit of the subtraction amplifier 14)

$= (VIN_{p-p}/4) (- (3VIN_{p-p}/16))$ In the $x2 = VIN_{p-p}/83$ step circuit 5, the same operation as the 2nd step of circuit 4 is performed to the output of the subtraction amplifier 14 of the 2nd step of circuit 3. Thereby, a 2-bit digital output ($2^3, 2^2$) is obtained at least for Nakashita from the 3rd step of circuit 5. The output voltage range of each part is the same as that of the 2nd step of circuit 4.

[0018] In the 4th step of circuit 6, sub A/D converter 9 performs an A/D conversion to the output of the subtraction amplifier 14 of the 3rd step of circuit 5, and the digital output ($2^1, 2^0$) of 2 bits of low ranks is obtained.

[0019] The digital output of the 1st step – the 4th step of circuits 3–6 arrives at the output circuit 8 simultaneously through each latch circuitry 7. That is, each latch circuitry 7 is formed in order to take the synchronization of the digital output of each circuits 3–6.

[0020] The output circuit 8 carries out the after [a digital compensation process] parallel output of the 10-bit digital output Dout of the analog input signal Vin, when required.

[0021] Thus, even if the conversion number of bits increases and LSB (Least Significant Bit) becomes small with reduction in power supply voltage, the resolution of sub A/D converter 9 can be raised and sufficient conversion precision is acquired.

[0022] Drawing 24 (a) is a figure for the circuit diagram and drawing 24 (b) in which the composition of the subtraction amplifier of the analog-to-digital circuit of drawing 23 is shown to explain operation of the subtraction amplifier of drawing 24 (a).

[0023] In drawing 24, the inversed input terminal of the operational amplifier 101 is connected to the node nb, and the non-inversed input terminal is grounded. The output terminal of the operational amplifier 101 is connected to the inversed input terminal via the capacitor 102 while being connected to the node no. Switch SW1 is connected between the inversed input terminal of the operational amplifier 1, and a non-inversed input terminal, and the capacitor 103 is connected between the node nb and the node na. It is connected to the node n1 via switch SW2, and the node na is connected to the node n2 via switch SW3. These switch SW2 and SW3 are constituted by the CMOS switch which usually consists of a CMOS (complementary-type metal oxide semiconductor) field effect transistor.

[0024] Voltage V_1 is inputted into the node n1, voltage V_2 is inputted into the node n2, and voltage V_O is outputted from the node no.

[0025] Here, operation of the subtraction amplifier of drawing 24 (a) is explained, referring to drawing 24 (b). Capacity value of the capacitor 101 is set to C, capacity value of the capacitor 103 is set to KC, and earth potentials are made into V_G . K is a constant.

[0026] First, switch SW1 and switch SW2 are made one, and switch SW3 is turned OFF. Thereby, the voltage of the node na serves as V_1 . The voltage of the node no is set to 0. At this time, the electric charge Qa of the node nb becomes like a following formula.

[0027] After turning OFF Qa= $(V_G - V_1) KC$, next switch SW1, switch SW2 is turned OFF and switch SW3 is made one. Thereby, the voltage of the node na serves as V_2 . The voltage of the node no serves as V_O . In order to carry out the imaginary earth of the node nb at this time, the electric charge Qb of the node nb becomes like a following formula.

[0028] Since there is no course out of which an electric charge escapes from and comes in the Qb= $(V_G - V_2) KC + (V_G - V_O) C$ node nb, it becomes Qa=Qb with conservation of charge. Therefore, a following formula is materialized.

[0029] $(V_G - V_1)$ Voltage V_O of a $KC = (V_G - V_2) KC + (V_G - V_O) C$ top type to the node no becomes like a following formula.

[0030] Voltage V_2 is subtracted from $V_O = V_G + (V_1 - V_2) K$, thus voltage V_1 , and the subtraction value is amplified K times.

[0031] Therefore, a subtraction amplifier has a function which outputs the difference of voltage

V_1 and voltage V_2 by the profit decided by the capacity factor of the capacitor 103 and the capacitor 102. For example, a sample hold function 1 time the profit of this will be given to a subtraction amplifier by setting it as $KC=C$ ($K=1$).

[0032] Drawing 25 is a figure showing the composition of the sub A/D converter used in the analog-to-digital circuit of drawing 23.

[0033] Two or more comparators 900 are arranged in the parallel connected type analog-digital converter 9 of drawing 25. The analog input voltage V_{in} is given to one input terminal of two or more comparators 900, and the reference voltage obtained by carrying out the partial pressure of the voltage between the high potential side reference voltage V_{RT} and the low voltage side reference voltage V_{RB} to the input terminal of another side by two or more resistance R is given, respectively. Each comparator 900 compares the voltage of one input terminal with the voltage of the input terminal of another side. The digital code D_{code} can be obtained by encoding the comparison result of two or more comparators 900 with the encoder 910.

[0034] By the way, when the voltage range of the analog input signal given to an analog-to-digital circuit is changed, Or to change the method of the analog input signal given to an analog-to-digital circuit in a differential double end input and a single-ended input, it is necessary to change the specification of an analog-to-digital circuit.

[0035] Here, a differential double end input and a single-ended input are explained. Drawing 26 (a) and (b) is a figure for explaining the analog to digital in a differential double end input and a single-ended input. A horizontal axis shows the analog input voltage V_{IN} , and a vertical axis shows the outputted digital code D_{code} .

[0036] As shown in drawing 26 (a), at the time of a differential double end input, the right side analog input voltage V_{in} (+) and the negative side analog input voltage V_{in} (-) of the analog input signal V_{in} change complementarily. Thereby, the difference of the right side analog input voltage V_{in} (+) and the negative side analog input voltage V_{in} (-) serves as voltage range $V_{IN_{p-p}}$ of the analog input signal V_{in} .

[0037] Therefore, as shown in drawing 26 (a), the right side analog input voltage V_{in} (+) changes from 1.0V in 2.0, When the negative side analog input voltage V_{in} (-) changes in 2.0V to 1.0V, the voltage range of the analog input signal V_{in} is set to 2.0V from the operation of $V_{in}(+)-V_{in}(-)$.

[0038] On the other hand, as shown in drawing 26 (b), at the time of a single-ended input, the right side analog input voltage V_{in} (+) changes. Thereby, the voltage range of the right side analog input voltage V_{in} (+) turns into a voltage range of the analog input signal V_{in} .

[0039] Therefore, as shown in drawing 26 (b), when the right side analog input voltage V_{in} (+) changes in 1.0V to 2.0V, the voltage range of an analog input signal is set to 1.0V.

[0040] That is, if the voltage range of the analog input signal V_{in} of a differential double end input method is made into $2V_{IN_{p-p}}$, the voltage range of the analog input signal V_{in} of a single-ended input method will serve as $V_{IN_{p-p}}$.

[0041] Thus, with a differential double end input method and a single-ended input method, even if the range of change of each analog input voltage is the same, the voltage ranges of an analog input signal will differ.

[0042] In the above-mentioned conventional analog-to-digital circuit, when changing the voltage range of an analog input signal, or when changing the input method of an analog input signal, it is necessary to redesign circuitry.

[0043] The purpose of this invention is to provide the pipeline type analog-to-digital circuit which can change the input method between change of the voltage range of an analog input signal or a differential double end input, and a single-ended input easily without redesigning circuitry.

[0044]

[The means for solving a technical problem and an effect of the invention] (1) The analog-to-digital circuit concerning the 1st invention invention of the 1st, Have the multi stage pipeline constitution which consists of two or more steps of circuits, and the circuit of each stage except the circuit of a final stage, The analog-digital converter which changes the inputted analog signal into a digital signal, The digital-to-analog converter which changes into an analog

signal the digital signal outputted from an analog-digital converter, Have the 1st arithmetic amplifier that amplifies the difference of the analog signal inputted and the analog signal outputted from a digital-to-analog converter, and the circuit of a final stage, The analog-digital converter which changes the inputted analog signal into a digital signal is included, The analog-digital converter which has a switching means from which at least one step of circuit except the circuit of a final stage changes a full-scale range to two or more steps, At least one of the 1st arithmetic amplifiers that have a switching means which changes the digital-to-analog converter and profit which have a switching means which changes a full-scale range to two or more steps to two or more steps is included, And/or, the circuit of a final stage contains the analog-digital converter which has a switching means which changes a full-scale range to two or more steps.

[0045]In an analog-to-digital circuit concerning this invention, An analog-digital converter which has a switching means from which at least one step of circuit except a circuit of a final stage changes a full-scale range to two or more steps, At least one of the 1st arithmetic amplifiers that have a switching means which changes a digital-to-analog converter and a profit which have a switching means which changes a full-scale range to two or more steps, and to change to two or more steps is included, And/or, since a circuit of a final stage contains an analog-digital converter which has a switching means which changes a full-scale range to two or more steps, At least one of a full-scale range of an analog-to-digital circuit, a full-scale range of a digital-to-analog converter, and profits of the 1st arithmetic amplifier can be changed.

[0046]Redesign of circuitry becomes unnecessary even if a voltage range of an analog input signal is changed by that cause by changing a differential double end input method into a single-ended input method. Redesign of circuitry becomes unnecessary, when changing a voltage range of an analog input signal of a single-ended input, or also when changing a voltage range of an analog input signal of a differential double end input.

[0047]Therefore, an input method between change of a voltage range of an analog input signal or a differential double end input, and a single-ended input can be changed easily, without redesigning circuitry.

[0048]As a result, while being able to attain shortening of a development cycle of an analog-to-digital circuit, low power consumption can be easily performed by optimizing optimization of a voltage range.

[0049](2) An analog-to-digital circuit concerning the 2nd invention invention of the 2nd, In composition of an analog-to-digital circuit concerning the 1st invention, a circuit of each stage except a circuit of a final stage, The 2nd arithmetic amplifier of at least one step of circuit except a circuit of a final stage has a switching means which changes a profit to two or more steps, including further the 2nd arithmetic amplifier that amplifies an inputted analog signal and is given to the 1st arithmetic amplifier.

[0050]In this case, by changing a profit of the 2nd arithmetic amplifier of at least one step of circuit to two or more steps, It becomes possible to change an input method between change of a voltage range of an analog input signal or a differential double end input, and a single-ended input easily, without redesigning circuitry.

[0051](3) In composition of an analog-to-digital circuit which an analog-to-digital circuit concerning the 3rd invention invention of the 3rd requires for the 1st or 2nd invention, the 1st arithmetic amplifier of at least one step of circuit except a circuit of a final stage has a switching means which changes a profit to two or more steps.

[0052]In this case, by changing a profit of the 1st arithmetic amplifier of at least one step of circuit to two or more steps, It becomes possible to change an input method between change of a voltage range of an analog input signal or a differential double end input, and a single-ended input easily, without redesigning circuitry.

[0053](4) An analog-to-digital circuit concerning the 4th invention invention of the 4th, In composition of an analog-to-digital circuit concerning the 1st - the 3rd one of inventions, an analog-digital converter of at least one step of circuit has a switching means which changes a full-scale range to two or more steps.

[0054]In this case, a full-scale range of an analog-digital converter of at least one step of circuit to two or more steps by switchable *****. It becomes possible to change an input method

between change of a voltage range of an analog input signal or a differential double end input, and a single-ended input easily, without redesigning circuitry.

[0055](5) An analog-to-digital circuit concerning the 5th invention invention of the 5th, In composition of an analog-to-digital circuit concerning the 1st – the 4th one of inventions, a digital-to-analog converter of at least one step of circuit except a circuit of a final stage has a switching means which changes a full-scale range to two or more steps.

[0056]In this case, by changing a full-scale range of a digital-to-analog converter of at least one step of circuit to two or more steps, It becomes possible to change an input method between change of a voltage range of an analog input signal or a differential double end input, and a single-ended input easily, without redesigning circuitry.

[0057](6) An analog-to-digital circuit concerning the 6th invention invention of the 6th, In composition of an analog-to-digital circuit concerning the 2nd invention, the 2nd arithmetic amplifier of at least one step of circuit, It has input capacitance, feedback capacity, and an operational amplifier, an inputted analog signal is amplified on a profit which becomes settled with a value of input capacitance, and a value of feedback capacity, and a switching means contains a variable region which sets either [at least] a value of input capacitance, or a value of feedback capacity as variable.

[0058]In this case, an inputted analog signal is amplified on a profit which becomes settled with a value of input capacitance, and a value of feedback capacity. Therefore, a profit of the 2nd arithmetic amplifier can be easily changed by changing either [at least] a value of input capacitance of an operational amplifier, or a value of feedback capacity.

[0059](7) In composition of an analog-to-digital circuit which requires an analog-to-digital circuit concerning invention the 7th invention of the 7th for the 6th invention, a variable region contains a switch part changed to a state or the state where it connected too hastily where a part of input capacitance or feedback capacity was separated.

[0060]In this case, input capacitance or feedback capacity of an operational amplifier can be changed by changing to a state or the state where it connected too hastily where a part of input capacitance or feedback capacity was separated by switch part. Thereby, a profit of the 2nd arithmetic amplifier can be changed easily.

[0061](8) An analog-to-digital circuit concerning the 8th invention invention of the 8th, In composition of an analog-to-digital circuit concerning the 3rd invention, the 1st arithmetic amplifier of at least one step of circuit, It has input capacitance, feedback capacity, and an operational amplifier, an inputted analog signal is amplified on a profit which becomes settled with a value of input capacitance, and a value of feedback capacity, and a switching means contains a variable region which sets either [at least] a value of input capacitance, or a value of feedback capacity as variable.

[0062]In this case, an inputted analog signal is amplified on a profit which becomes settled with a value of input capacitance, and a value of feedback capacity. Therefore, a profit of the 1st arithmetic amplifier can be easily changed by changing either [at least] a value of input capacitance of an operational amplifier, or a value of feedback capacity.

[0063](9) In composition of an analog-to-digital circuit which requires an analog-to-digital circuit concerning invention the 9th invention of the 9th for the 8th invention, a variable region contains a switch part changed to a state or the state where it connected too hastily where a part of input capacitance or feedback capacity was separated.

[0064]In this case, input capacitance or feedback capacity of an operational amplifier can be changed from changing to a state or the state where it connected too hastily where a part of input capacitance or feedback capacity was separated by switch part. Thereby, a profit of the 1st arithmetic amplifier can be changed easily.

[0065](10) An analog-to-digital circuit concerning the 10th invention invention of the 10th, In composition of an analog-to-digital circuit concerning the 9th invention, a switch part is connected to the 2nd capacity in series or in parallel including the 1st and 2nd capacity by which feedback capacity was provided in parallel or in series between an input terminal of an operational amplifier, and an output terminal.

[0066]If a switch part is made into a connected state, the 1st and 2nd capacity will be

connected in parallel or in series between an input terminal of an operational amplifier, and an output terminal. Thereby, feedback capacity increases or decreases. If a switch part is made into a cut off state, only the 1st capacity will be connected between an input terminal of an operational amplifier, and an output terminal. Thereby, feedback capacity decreases or increases.

[0067](11) A switch part is connected to an output terminal of an operational amplifier in composition of an analog-to-digital circuit which requires an analog-to-digital circuit concerning invention the 11th invention of the 11th for the 10th invention.

[0068]When the 2nd capacity is connected to an output side rather than a switch part, even if a switch part is set as a cut off state, parasitic capacitance of the 2nd capacity is charged. By that cause, it will be necessary to take parasitic capacitance into consideration, and a profit will vary with dispersion in parasitic capacitance at the time of setting out of a profit. Here, by connecting a switch part to an output side rather than the 2nd capacity, when a switch part is set as a cut off state, the 2nd capacity is separated from an output terminal by switch part with parasitic capacitance. Therefore, it becomes unnecessary to take parasitic capacitance of the 2nd capacity into consideration at the time of setting out of a profit, and dispersion in a profit by dispersion in parasitic capacitance is lost.

[0069](12) In composition of an analog-to-digital circuit which requires an analog-to-digital circuit concerning invention the 12th invention of the 12th for the 9th invention, input capacitance is provided in an input terminal of an operational amplifier in parallel or in series.

[0070]If a switch part is made into a connected state, the 1st and 2nd capacity will be connected to an input terminal of an operational amplifier in parallel or in series. Thereby, input capacitance increases or decreases. Only the 1st capacity will be connected to an input terminal of an operational amplifier if a switch part is made into a cut off state. Thereby, input capacitance decreases or increases.

[0071](13) A switch part is connected to an input side of the 2nd capacity in composition of an analog-to-digital circuit which requires an analog-to-digital circuit concerning invention the 13th invention of the 13th for the 12th invention.

[0072]When the 2nd capacity is connected to an input side rather than a switch part, even if a switch part is set as a cut off state, parasitic capacitance of the 2nd capacity is charged. By that cause, it will be necessary to take parasitic capacitance into consideration, and a profit will vary with dispersion in parasitic capacitance at the time of setting out of a profit. Here, by connecting a switch part to an input side rather than the 2nd capacity, when a switch part is set as a cut off state, it is separated from a node in which the 2nd capacity receives an input signal by a switch part with parasitic capacitance. Therefore, it becomes unnecessary to take parasitic capacitance of the 2nd capacity into consideration at the time of setting out of a profit, and dispersion in a profit by dispersion in parasitic capacitance is lost.

[0073](14) An analog-to-digital circuit concerning the 14th invention invention of the 14th, In composition of an analog-to-digital circuit concerning the 4th invention, an analog-digital converter of at least one step of circuit, A switching means contains a variable region which sets as variable two or more reference voltage generated by circuit generating reference voltage including circuit generating reference voltage which generates two or more reference voltage, and two or more comparators compared with an analog signal into which two or more reference voltage generated by circuit generating reference voltage was inputted.

[0074]In this case, a voltage range of reference voltage can be changed by changing reference voltage generated by circuit generating reference voltage. Thereby, a full-scale range of an analog-digital converter can be changed easily.

[0075](15) An analog-to-digital circuit concerning the 15th invention invention of the 15th, In composition of an analog-to-digital circuit concerning the 5th invention, a digital-to-analog converter of at least one step of circuit except a circuit of a final stage, Circuit generating reference voltage which generates reference voltage, and two or more capacity connected to a common terminal, Two or more switches which give reference voltage which was connected between circuit generating reference voltage and two or more capacity, and was generated by circuit generating reference voltage according to a digital signal inputted to two or more

capacity, respectively are included, A switching means contains a variable region which sets reference voltage generated by circuit generating reference voltage as variable.

[0076] In this case, a voltage range of reference voltage can be changed by changing reference voltage generated by circuit generating reference voltage. Thereby, a full-scale range of a digital-to-analog converter can be changed easily.

[0077]

[Embodiment of the Invention](1) The 1st embodiment drawing 1 is a block diagram showing the composition of the pipeline type analog-to-digital circuit in a 1st embodiment of this invention. The analog-to-digital circuit of drawing 1 has 10-bit four-step pipeline constitution.

[0078] In drawing 1, the analog-to-digital circuit 1 comprises the circuits 3-6, two or more latch circuitry 7, and the output circuit 8 of the 2 or 1st step - the 4th step of sample hold circuit.

[0079] The 1st (first rank) step of circuit 3 is provided with the arithmetic amplifier 11a, the subtractor circuit 12, and the arithmetic amplifier 13 which have sub A/D converter 9a which has a switchable full-scale range, D/A converter 10, and a switchable profit. The subtractor circuit 12 and the arithmetic amplifier 13 constitute the subtraction amplifier 14. The 2nd step and the 3rd step of circuits 4 and 5 are provided with sub A/D converter 9, D/A converter 10, the arithmetic amplifier 11, the subtractor circuit 12, and the arithmetic amplifier 13. The subtractor circuit 12 and the arithmetic amplifier 13 constitute the subtraction amplifier 14. The 4th (final stage) step of circuit 6 is provided only with sub A/D converter 9.

[0080] That the pipeline type analog-to-digital circuit 1 of drawing 1 differs from the conventional analog-to-digital circuit 100 of drawing 20, It is the point that the arithmetic amplifier 11a which has sub A/D converter 9a and the switchable profit which have a switchable full-scale range is used for the 1st step of circuit 3.

[0081] Here, the full-scale range of sub A/D converter 9 in the 1st step of circuit 3, It changes to voltage range $V_{IN_{p-p}}$ equal to it when the voltage range of an analog input signal is $V_{IN_{p-p}}$, and when the voltage ranges of an analog input signal are $V_{IN_{p-p}}/2$, it changes to voltage range $V_{IN_{p-p}}/2$. [equal to it] The profit of the arithmetic amplifier 11a in the 1st step of circuit 3 is changed 1 time, when the voltage range of an analog input signal is $V_{IN_{p-p}}$, and when the voltage ranges of an analog input signal are $V_{IN_{p-p}}/2$, it is changed twice.

[0082] The full-scale range of D/A converter 10 in the 1st step - the 3rd step of circuit 3-5 is fixed, and the full-scale range of sub A/D converter 9 in the 2nd step - the 4th step of circuit 4-6 is being fixed. The profit of the arithmetic amplifiers 11 and 13 in the arithmetic amplifier 13 in the 1st step of circuit 3, the 2nd step, and the 3rd step of circuit 3 and 4 is 2.

[0083] 4 bit configurations and the 2-4th step of circuits 4-6 of the 1st step of circuit 3 are 2 bit configurations, respectively. Similarly in the 1-3rd step of circuits 3-5, the number of bits (bit configuration) of sub A/D converters 9 and 9a and D/A converter 10 is set up.

[0084] Operation of the analog-to-digital circuit 1 of drawing 1 in case the voltage range of an analog input signal is $V_{IN_{p-p}}$, and the voltage range of each part are the same as that of the analog-to-digital circuit 100 of drawing 20.

[0085] Here, operation of the analog-to-digital circuit 1 of drawing 1 in case the voltage ranges of an analog input signal are $V_{IN_{p-p}}/2$, and the output voltage range of each part are explained.

[0086] The sample hold circuit 2 samples the analog input signal V_{in} , and carries out fixed time maintenance. The analog input signal V_{in} outputted from the sample hold circuit 2 is transmitted to the 1st step of circuit 3.

[0087] In the 1st step of circuit 3, sub A/D converter 9a performs an analog to digital to the analog input signal V_{in} of voltage range $V_{IN_{p-p}}/2$. The full-scale range of sub A/D converter 9a at this time is changed to $V_{IN_{p-p}}/2$ as mentioned above.

[0088] Top 4-bit digital output ($2^9, 2^8, 2^7, 2^6$) which is an A/D conversion result of sub A/D converter 9a is transmitted to the output circuit 8 via the four latch circuitry 7 while it is transmitted to D/A converter 10. D/A converter 10 changes into an analog signal top 4-bit digital output which is an A/D conversion result of sub A/D converter 9a.

[0089] Since the full-scale range of D/A converter 10 is being fixed to VIN_{p-p} , the normal output voltage range of D/A converter 10 is expressed like a following formula.

[0090]

(The 1st step of resolution-1) \times (full-scale range of D/A converter 10) / (the 1st step of resolution)

$= (2^4 - 1) \times (VIN_{p-p}) / 2^4 = 15VIN_{p-p} / 16$ one side and the arithmetic amplifier 11a sample the analog input signal Vin , and amplify and hold it. As mentioned above, since a profit is changed twice when the voltage ranges of an analog input signal are $VIN_{p-p} / 2$, the output voltage range of the arithmetic amplifier 11a is expressed like a following formula.

[0091]

(Voltage range of the analog input signal Vin) \times (profit of the arithmetic amplifier 11a)

$= (VIN_{p-p} / 2) \times 2 = VIN_{p-p}$ subtraction amplifier 14 subtracts and amplifies the analog input signal Vin and the D/A conversion result of D/A converter 10 which were outputted from the arithmetic amplifier 11a. The output of the subtraction amplifier 14 is transmitted to the 2nd step of circuit 4.

[0092] The output voltage range of the 1st step of subtraction amplifier 14 is expressed like a following formula.

(Output voltage range of the arithmetic amplifier 11a) \times (- (normal output voltage range of D/A converter 10)) (profit of the subtraction amplifier 14)

$= (VIN_{p-p}) \times (- (15VIN_{p-p} / 16))$ In the $\times 2 = VIN_{p-p} / 82$ step circuit 4, sub A/D converter 9 performs an A/D conversion to the output of the subtraction amplifier 14 of the 1st step of circuit 3. The A/D conversion result of sub A/D converter 9 is transmitted to the output circuit 8 via the three latch circuitry 7 while it is transmitted to D/A converter 10. Thereby, a 2-bit digital output ($2^5, 2^4$) is obtained at least for Nakagami from the 2nd step of circuit 4.

[0093] On the other hand, the arithmetic amplifier 11 amplifies the output of the subtraction amplifier 14 of the 1st step of circuit 3. The subtraction amplifier 14 subtracts and amplifies the output of the arithmetic amplifier 11, and the D/A conversion result of D/A converter 10. The output of the subtraction amplifier 14 is transmitted to the 3rd step of circuit 5.

[0094] In the 3rd step of circuit 5, the same operation as the 2nd step of circuit 4 is performed to the output of the subtraction amplifier 14 of the 2nd step of circuit 4. Thereby, a 2-bit digital output ($2^3, 2^2$) is obtained at least for Nakashita from the 3rd step of circuit 5.

[0095] In the 4th step of circuit 6, sub A/D converter 9 performs an A/D conversion to the output of the subtraction amplifier 14 of the 3rd step of circuit 5, and the digital output ($2^1, 2^0$) of 2 bits of low ranks is obtained.

[0096] The digital output of the 1st step - the 4th step of circuits 3-6 arrives at the output circuit 8 simultaneously through each latch circuitry 7. That is, each latch circuitry 7 is formed in order to take the synchronization of the digital output of each circuits 3-6.

[0097] The output circuit 8 carries out the after [a digital compensation process] parallel output of the 10-bit digital output $Dout$ of the analog input signal Vin , when required.

[0098] As mentioned above, when the voltage ranges of an analog input signal are $VIN_{p-p} / 2$. By changing the full-scale range of the profit of the arithmetic amplifier 11a of the 1st step of circuit 3, and sub A/D converter 9a of the 1st step of circuit 3, The voltage range of the output signal given in the 2nd step of circuit 5 is set to $VIN_{p-p} / 8$ from the subtraction amplifier 14 of the 1st step of circuit 3 like the case where the voltage range of an analog input signal is VIN_{p-p} . Thereby, although the voltage range of the analog input signal Vin became half, the digital output same before the voltage range of an analog input signal becomes half is obtained.

[0099] Therefore, the analog-to-digital circuit corresponding to change of the voltage range of an analog input signal can be provided, without changing a circuit design.

[0100] According to this embodiment, the analog-to-digital circuit of a differential double end input method can be changed into the analog-to-digital circuit of a single-ended input method,

without changing circuitry.

[0101]Drawing 2 (a) and (b) is a figure showing setting out in the case of changing the analog-to-digital circuit 1 of drawing 1 to a differential double end input method and a single-ended input method, respectively.

[0102]As shown in drawing 2 (a), at the time of a differential double end input, the profit of the arithmetic amplifier 11a is changed 1 time, and the full-scale range of sub A/D converter 9a is changed to $2VIN_{p-p}$. In this example, the right side analog input voltage V_{in} of the analog input signal V_{in} of a differential double end input (+) changes in 1.0V to 2.0V, and the negative side analog input voltage V_{in} (-) changes from 2.0V in 1.0V. The voltage range of the analog input signal V_{in} becomes like a following formula.

[0103]The maximum of $2VIN_{p-p} = \{V_{in}(+) - V_{in}(-)\} - \text{minimum} = 2.0 \text{ [V]}$ of $\{V_{in}(+) - V_{in}(-)\}$

In this case, the right side reference voltage V_{ref} of sub A/D converter 9a (+) changes in 1.0V to 2.0V, and the negative side reference voltage V_{ref} (-) changes from 2.0V in 1.0V.

[0104]As shown in drawing 2 (b), at the time of a single-ended input, the profit of the arithmetic amplifier 11a is changed twice, and the full-scale range of sub A/D converter 9a is changed to VIN_{p-p} . The right side analog input voltage V_{in} of the analog input signal V_{in} of the single-ended input in this example (+) changes in 1.0V to 2.0V, and that of the negative side analog input voltage V_{in} (-) is constant 1.5V. The voltage range of the analog input signal V_{in} becomes like a following formula.

[0105]The maximum of $VIN_{p-p} = \{V_{in}(+) - V_{in}(-)\} - \text{minimum} = 1.0 \text{ [V]}$ of $\{V_{in}(+) - V_{in}(-)\}$

In this case, the right side reference voltage V_{ref} of sub A/D converter 9a (+) changes in 1.0V to 2.0V, and its negative side reference voltage V_{ref} (-) is constant 1.5V.

[0106]Thus, in the analog-to-digital circuit 1 of drawing 1, even if the voltage range of an analog input signal is set to one half by changing a differential double end input method into a single-ended input method, redesign of circuitry becomes unnecessary.

[0107]Redesign of circuitry becomes unnecessary, when changing the voltage range of the analog input signal of a single-ended input into one half, and also when changing the voltage range of the analog input signal of a differential double end input into one half.

[0108]Thus, in the same LSI (large scale integration circuit), the voltage range of the output of an analog input signal and an arithmetic amplifier, the output of a D/A conversion circuit, and the output of a subtraction amplifier can be changed programmably. As a result, while being able to attain shortening of a development cycle, it is also possible to perform low power consumption.

[0109](2) The 2nd embodiment drawing 3 is a block diagram showing the composition of the pipeline type analog-to-digital circuit in a 2nd embodiment of this invention. The analog-to-digital circuit 1 of drawing 3 also has 10-bit four-step pipeline constitution.

[0110]In drawing 3, the analog-to-digital circuit 1 comprises the circuits 3-6, two or more latch circuitry 7, and the output circuit 8 of the 2 or 1st step - the 4th step of sample hold circuit.

[0111]4 bit configurations and the 2-4th step of circuits 4-6 of the 1st step of circuit 3 are 2 bit configurations, respectively. Similarly in the 1-3rd step of circuits 3-5, the number of bits (bit configuration) of sub A/D converters 9 and 9b and D/A converters 10 and 10b is set up.

[0112]The 1st (first rank) step of circuit 3 is provided with the arithmetic amplifier 13a which has sub A/D converter 9, D/A converter 10, the arithmetic amplifier 11, the subtractor circuit 12, and a switchable profit. The subtractor circuit 12 and the arithmetic amplifier 13a constitute the subtraction amplifier 14a.

[0113]The 2nd step and the 3rd step of circuits 4 and 5 are provided with sub A/D converter 9b which has a switchable full-scale range, D/A converter 10b which has a switchable full-scale range, the arithmetic amplifier 11, the subtractor circuit 12, and the arithmetic amplifier 13. The subtractor circuit 12 and the arithmetic amplifier 13 constitute the subtraction amplifier 14. The 4th (final stage) step of circuit 6 is provided only with sub A/D converter 9b which has a switchable full-scale range.

[0114]Here, the 2nd step - the 4th step of sub A/D converter 9b shall have the 2nd step - the 4th step of A/D converter 9 of drawing 20 twice the accuracy of sub. Redesign of the analog-

to-digital circuit 1 at the time of using for the 2nd step – the 4th step hereafter sub A/D converter 9b which has twice as many accuracy as this is explained.

[0115]It is switchable 1 time and twice in the profit of the subtraction amplifier 14a in the 1st step of circuit 3. It is switchable to $VIN_{p-p}/8$, and $VIN_{p-p}/16$ in the full-scale range of sub A/D converter 9b in the 2nd step – the 4th step of circuit 4–6. It is switchable to $VIN_{p-p}/4$, and $VIN_{p-p}/8$ in the full-scale range of D/A converter 10b in the 2nd step and the 3rd step of circuit 4 and 5.

[0116]Here, the profit of the subtraction amplifier 14a in the 1st step of circuit 3 is changed 1 time. The full-scale range of sub A/D converter 9b in the 2nd step – the 4th step of circuit 4–6 is changed to $VIN_{p-p}/16$, and the full-scale range of D/A converter 10b in the 2nd step and the 3rd step of circuit 4 and 5 is changed to $VIN_{p-p}/8$. The full-scale range of sub A/D converter 9 in the 1st step of circuit 3 is VIN_{p-p} . The profit of the arithmetic amplifiers 11 and 13 in the 2nd step and the 3rd step of circuit 3 and 4 is 2.

[0117]Here, operation of the analog-to-digital circuit 1 of drawing 1 in case the voltage range of an analog input signal is VIN_{p-p} , and the output voltage range of each part are explained.

[0118]The sample hold circuit 2 samples the analog input signal Vin , and carries out fixed time maintenance. The analog input signal Vin outputted from the sample hold circuit 2 is transmitted to the 1st step of circuit 3.

[0119]In the 1st step of circuit 3, sub A/D converter 9 performs an analog to digital to the analog input signal Vin of voltage range VIN_{p-p} . The full-scale range of sub A/D converter 9 at this time is VIN_{p-p} .

[0120]Top 4-bit digital output ($2^9, 2^8, 2^7, 2^6$) which is an A/D conversion result of sub A/D converter 9 is transmitted to the output circuit 8 via the four latch circuitry 7 while it is transmitted to D/A converter 10. D/A converter 10 changes into an analog signal top 4-bit digital output which is an A/D conversion result of sub A/D converter 9.

[0121]Since the full-scale range of D/A converter 10 is being fixed, the normal output voltage range of D/A converter 10 is expressed like a following formula.

[0122]

(The 1st step of resolution-1) x(full-scale range of D/A converter 10)/(the 1st step of resolution)

$= (2^4 - 1) \times (VIN_{p-p}) / 2^4 = 15VIN_{p-p}/16$ one side and the arithmetic amplifier 11 sample the analog input signal Vin , and amplify and hold it. Since the profit of the arithmetic amplifier 11 is 1 time, the output voltage range of the arithmetic amplifier 11 is expressed like a following formula.

[0123]

(Voltage range of the analog input signal Vin) x (profit of the arithmetic amplifier 11)

$= \text{The } VIN_{p-p} \times 1 = VIN_{p-p}$ subtraction amplifier 14a subtracts and amplifies the analog input signal Vin and the D/A conversion result of D/A converter 10 which were outputted from the arithmetic amplifier 11. The output of the subtraction amplifier 14a is transmitted to the 2nd step of circuit 4.

[0124]Since the profit of the 1st step of subtraction amplifier 14a is changed to 1, the output voltage range of the 1st step of subtraction amplifier 14a is expressed like a following formula.

[0125]

(Output voltage range of the arithmetic amplifier 11) x (– (normal output voltage range of D/A converter 10)) (profit of the subtraction amplifier 14a)

$= (VIN_{p-p}) (- (15VIN_{p-p}/16))$ In the $\times 1 = VIN_{p-p}/16$ 2nd step circuit 4, sub A/D converter 9b performs an A/D conversion to the output of the subtraction amplifier 14a of the 1st step of circuit 3. The A/D conversion result of sub A/D converter 9b is transmitted to the output circuit 8 via the three latch circuitry 7 while it is transmitted to D/A converter 10b.

[0126]In this case, since sub A/D converter 9b has A/D converter 9 of drawing 20 twice the accuracy of sub, A 2-bit digital output ($2^5, 2^4$) is obtained at least for Nakagami from the 2nd step of circuit 4 by full-scale range $VIN_{p-p}/16$ of the half of sub A/D converter 9 of drawing 20.

[0127]At least Nakagami whose D/A converter 10b is an A/D conversion result of sub A/D converter 9b changes a 2-bit digital output into an analog signal.

[0128]Since the full-scale range of D/A converter 10b is changed to $VIN_{p-p}/8$ of the half of D/A converter 10 of drawing 20, the normal output voltage range of D/A converter 10b is expressed like a following formula.

[0129]

(The 2nd step of resolution-1) x (full-scale range of D/A converter 10b)
/(the 2nd step of resolution)

$= (2^2 - 1) \times (VIN_{p-p}/8) / 2^2 = 3VIN_{p-p}/32$ one side and the arithmetic amplifier 11 amplify the output of the subtraction amplifier 14a of the 1st step of circuit 3. As mentioned above, since the profit of the subtraction amplifier 14a of the 1st step of circuit 3 is changed to 1, the output voltage range of the arithmetic amplifier 11a is expressed like a following formula.

[0130]

(Output voltage range of the 1st step of subtraction amplifier 14a) x (profit of the arithmetic amplifier 11)

$= (VIN_{p-p}/16) \times 2 = VIN_{p-p}/8$ subtraction amplifier 14 subtracts and amplifies the output of the arithmetic amplifier 11, and the D/A conversion result of D/A converter 10b. The output of the subtraction amplifier 14 is transmitted to the 3rd step of circuit 5.

[0131]The output voltage range of the 2nd step of subtraction amplifier 14 is expressed like a following formula.

(Output voltage range of the arithmetic amplifier 11) x (- (normal output voltage range of D/A converter 10b)) (profit of the subtraction amplifier 14)

$= (VIN_{p-p}/8) \times (- (3VIN_{p-p}/32))$ In the $x2 = VIN_{p-p}/163$ step circuit 5, the same operation as the 2nd step of circuit 4 is performed to the output of the subtraction amplifier 14 of the 2nd step of circuit 4. In this case, since sub A/D converter 9b has A/D converter 9 of drawing 20 twice the accuracy of sub, A 2-bit digital output ($2^3, 2^2$) is obtained at least for Nakashita from the 3rd step of circuit 5 by full-scale range $VIN_{p-p}/16$ of the half of sub A/D converter 9 of drawing 20.

The output voltage range of each part is the same as that of the 2nd step of circuit 4.

[0132]In the 4th step of circuit 6, sub A/D converter 9b performs an A/D conversion to the output of the subtraction amplifier 14 of the 3rd step of circuit 5. In this case, since sub A/D converter 9b has A/D converter 9 of drawing 20 twice the accuracy of sub, The digital output ($2^1, 2^0$) of 2 bits of low ranks is obtained from the 4th step of circuit 6 by full-scale range $VIN_{p-p}/16$ of the half of sub A/D converter 9 of drawing 20.

[0133]The digital output of the 1st step - the 4th step of circuits 3-6 arrives at the output circuit 8 simultaneously through each latch circuitry 7. That is, each latch circuitry 7 is formed in order to take the synchronization of the digital output of each circuits 3-6.

[0134]The output circuit 8 carries out the after [a digital compensation process] parallel output of the 10-bit digital output Dout of the analog input signal Vin, when required.

[0135]As mentioned above, in the analog-to-digital circuit 1 of drawing 3. Although the voltage range of each part of the circuits 4-6 after the 2nd step became half [of the analog-to-digital circuit 100 of drawing 20] by using sub A/D converter 9b which has twice as many accuracy as this, the digital output same before a voltage range becomes half is obtained.

[0136]In this case, the alternating current component of current which flows through the circuits 3-6 of each stage decreases by optimizing a voltage range to sub A/D converter 9b which has twice as many accuracy as this, and setting it as a half. Thereby, the consumed electric current can provide the analog-to-digital circuit by which reduction was carried out by optimizing a voltage range, without changing a circuit design.

[0137](3) Circuitry drawing 4 of each part is a circuit diagram showing the 1st example of the composition of the arithmetic amplifier 11a in the analog-to-digital circuit 1 of drawing 1.

[0138]The arithmetic amplifier 11a of drawing 4 includes the operational amplifier 110, the capacity value switching circuit 111,112, the capacitor 113,114, and the switches 115-122. The switches 115-122 are constituted by the MOS (metal oxide semiconductor) transistor, for example.

[0139]The capacity value switching circuit 111 is connected as feed back capacity between the inversed input terminal of the operational amplifier 110, and an inverted output terminal, and the capacity value switching circuit 112 is connected as feed back capacity between the non-inversed input terminal and the noninverting output terminal. The capacitor 113 is connected to the inversed input terminal of the operational amplifier 110 as input capacitance, and the capacitor 114 is connected to the non-inversed input terminal as input capacitance.

[0140]The right side analog input voltage $V_{in}(+)$ and middle reference voltage $VRT1$ are given to the capacitor 113 via the switch 115,116, respectively. The negative side analog input voltage $V_{in}(-)$ and middle reference voltage $VRT1$ are given to the capacitor 114 via the switch 117,118, respectively. The inversed input terminal, the inverted output terminal, non-inversed input terminal, and noninverting output terminal of the operational amplifier 110 are grounded via the switch 119,120,121,122, respectively.

[0141]If capacity value of the capacitor 113,114 is set to CA , respectively and capacity value of the capacity value switching circuit 111,112 is set to CB here, respectively, The right side analog output voltage V_o of the inverted output terminal of the operational amplifier 110 (+) and the negative side analog output voltage V_o of a noninverting output terminal (-) become like a following formula.

[0142]

$$V_o(+) = (V_{in}(+) - VRT1) \text{ and } (CA/CB)$$

$$V_o(-) = (V_{in}(-) - VRT1) \text{ and } (CA/CB)$$

$$\Delta V_o = V_o(+) - V_o(-)$$

$$= (V_{in}(+) - V_{in}(-)) - (CA/CB)$$

Therefore, the profit of the arithmetic amplifier 11a can be changed by changing the capacity value CB of the capacity value switching circuit 111,112.

[0143]Drawing 5 is a circuit diagram showing the 2nd example of the composition of the arithmetic amplifier 11a in the analog-to-digital circuit 1 of drawing 1.

[0144]The arithmetic amplifier 11a of drawing 5 includes the operational amplifier 110, the capacitor 123,124, the capacity value switching circuit 125,126, and the switches 115-122.

[0145]The capacitor 123 is connected as feed back capacity between the inversed input terminal of the operational amplifier 110, and an inverted output terminal, and the capacitor 124 is connected as feed back capacity between the non-inversed input terminal and the noninverting output terminal. The capacity value switching circuit 125 is connected to the inversed input terminal of the operational amplifier 110 as input capacitance, and the capacity value switching circuit 126 is connected to the non-inversed input terminal as input capacitance.

[0146]The right side analog input voltage $V_{in}(+)$ and middle reference voltage $VRT1$ are given to the capacity value switching circuit 125 via the switch 115,116, respectively. The negative side analog input voltage $V_{in}(-)$ and middle reference voltage $VRT1$ are given to the capacity value switching circuit 126 via the switch 117,118, respectively. The inversed input terminal, the inverted output terminal, non-inversed input terminal, and noninverting output terminal of the operational amplifier 110 are grounded via the switch 119,120,121,122, respectively.

[0147]If capacity value of the capacity value switching circuit 125,126 is set to CC , respectively and capacity value of the capacitor 123,124 is set to CD here, respectively, The right side analog output voltage V_o of the inverted output terminal of the operational amplifier 110 (+) and the negative side analog output voltage V_o of a noninverting output terminal (-) become like a following formula.

[0148]

$$V_o(+) = (V_{in}(+) - VRT1) \text{ and } (CC/CD)$$

$$V_o(-) = (V_{in}(-) - VRT1) \text{ and } (CC/CD)$$

$$\begin{aligned} \Delta V_o &= V_o(+)-V_o(-) \\ &= (V_{in}(+)-V_{in}(-)) - (CC/CD) \end{aligned}$$

Therefore, the profit of the arithmetic amplifier 11a can be changed by changing capacity value CC of the capacity value switching circuit 125,126.

[0149]Drawing 6 - drawing 11 are the circuit diagrams showing the 1st - the 6th example of the concrete circuitry of the arithmetic amplifier 11a.

[0150]In drawing 6 - drawing 11, each of the capacitors Ca, Cb, and Cc shall have the equal capacity value C. Let m be arbitrary positive integers.

[0151]In the example of drawing 6, the parallel circuit and the switch Sa of m capacitor Ca are connected in series between the inversed input terminal of the operational amplifier 110, and an inverted output terminal, and the parallel circuit of m capacitor Ca is connected. Here, m is arbitrary positive integers. Similarly, the parallel circuit and the switch Sa of m capacitor Ca are connected in series between the non-inversed input terminal of the operational amplifier 110, and a noninverting output terminal, and the parallel circuit of m capacitor Ca is connected. The 2m piece capacitor Cb is connected to the inversed input terminal of the operational amplifier 110, and the 2m piece capacitor Cb is connected to the non-inversed input terminal.

[0152]The right side analog input voltage Vin (+) is given to the 2m piece capacitor Cb by the side of an inversed input terminal via the switch S1, respectively. The negative side analog input voltage Vin (-) is given to the capacitor Cb by the side of a non-inversed input terminal via the switch S1, respectively. The high potential side reference voltage VRT is given to the m capacitors Cb by the side of an inversed input terminal, and the m capacitors Cb by the side of a non-inversed input terminal via the switch S2, respectively. The low voltage side reference voltage VRB is given to the m capacitors Cb by the side of a non-inversed input terminal, and the m capacitors Cb by the side of a non-inversed input terminal via the switch S2, respectively.

[0153]In this example, the values of input capacitance are 2mC. If the switch Sa is carried out to one, the value of feed back capacity will serve as 2mC, and if the switch Sa is turned OFF, the value of feed back capacity will serve as mC. Therefore, at the time of a differential double end input, by changing the switch Sa to one, a profit will be 1 time and a profit will be twice by changing the switch Sa to OFF at the time of a single-ended input.

[0154]In the example of drawing 7, the parallel circuit of 2m piece capacitor Ca and the parallel circuit of 2m piece capacitor Cc are connected in series between the inversed input terminal of the operational amplifier 110, and an inverted output terminal, and the switch Sa is connected in parallel with capacitor Cc. Similarly, the parallel circuit of 2m piece capacitor Ca and the parallel circuit of 2m piece capacitor Cc are connected in series between the non-inversed input terminal of the operational amplifier 110, and a noninverting output terminal, and the switch Sa is connected in parallel with capacitor Cc. The composition of other portions of the arithmetic amplifier 11a of drawing 7 is the same as that of the arithmetic amplifier 11a of drawing 6.

[0155]In this example, the values of input capacitance are 2mC. If the switch Sa is carried out to one, the value of feed back capacity will serve as 2mC, and if the switch Sa is turned OFF, the value of feed back capacity will serve as mC. Therefore, at the time of a differential double end input, by changing the switch Sa to one, a profit will be 1 time and a profit will be twice by changing the switch Sa to OFF at the time of a single-ended input.

[0156]In the example of drawing 8, the parallel circuit of 2m piece capacitor Ca and the parallel circuit of 2m piece capacitor Cc are connected in series between the inversed input terminal of the operational amplifier 110, and an inverted output terminal, and the switch Sa is connected in parallel with capacitor Ca. Similarly, the parallel circuit of 2m piece capacitor Ca and the parallel circuit of 2m piece capacitor Cc are connected in series between the non-inversed input terminal of the operational amplifier 110, and a noninverting output terminal, and the switch Sa is connected in parallel with capacitor Ca. The composition of other portions of the arithmetic amplifier 11a of drawing 8 is the same as that of the arithmetic amplifier 11a of drawing 6.

[0157]In this example, the values of input capacitance are 2mC. If the switch Sa is carried out to one, the value of feed back capacity will serve as 2mC, and if the switch Sa is turned OFF, the value of feed back capacity will serve as mC. Therefore, at the time of a differential double end

input, by changing the switch Sa to one, a profit will be 1 time and a profit will be twice by changing the switch Sa to OFF at the time of a single-ended input.

[0158]In the example of drawing 9, the parallel circuit of m capacitor Ca is connected between the inversed input terminal of the operational amplifier 110, and the inverted output terminal. Similarly, the parallel circuit of m capacitor Ca is connected between the non-inversed input terminal of the operational amplifier 110, and the noninverting output terminal. The 2m piece capacitor Cb is connected to the inversed input terminal of the operational amplifier 110, and the 2m piece capacitor Cb is connected to the non-inversed input terminal.

[0159]The right side analog input voltage Vin (+) is given to the 2m piece capacitor Cb by the side of an inversed input terminal via the switch S1 and S1a, respectively. The negative side analog input voltage Vin (-) is given to the capacitor Cb by the side of a non-inversed input terminal via the switch S1 and S1a, respectively. The high potential side reference voltage VRT is given to the m capacitors Cb by the side of an inversed input terminal, and the m capacitors Cb by the side of a non-inversed input terminal via the switch S2 and S2a, respectively. The low voltage side reference voltage VRB is given to the m capacitors Cb by the side of a non-inversed input terminal, and the m capacitors Cb by the side of a non-inversed input terminal via the switch S2 and S2a, respectively.

[0160]In this example, the value of feed back capacity is mC. If the switch S1a and S2a are made one, the value of input capacitance will serve as 2mC, and if the switch S1a and S2a are turned OFF, the value of input capacitance will serve as mC. Therefore, at the time of a differential double end input, by always turning OFF the switch S1a and S2a, a profit will be 1 time and a profit will be twice by carrying out switching operation of the switch S1a and the S2a like the switch S1 and S2 at the time of a single-ended input.

[0161]In the example of drawing 10, the parallel circuit of m capacitor Ca is connected between the inversed input terminal of the operational amplifier 110, and the inverted output terminal. Similarly, the parallel circuit of m capacitor Ca is connected between the non-inversed input terminal of the operational amplifier 110, and the noninverting output terminal. The parallel circuit of 2m piece capacitor Cc is connected to the inversed input terminal of the operational amplifier 110, the 2m piece capacitor Cb is connected to the parallel circuit of capacitor Cc, and the switch Sa is connected in parallel with capacitor Cc. The parallel circuit of 2m piece capacitor Cc is connected to a non-inversed input terminal, the 2m piece capacitor Cb is connected to the parallel circuit of capacitor Cc, and the switch Sa is connected in parallel with capacitor Cc. The composition of other portions of the arithmetic amplifier 11a of drawing 10 is the same as that of the arithmetic amplifier 11a of drawing 6.

[0162]In this example, the value of feed back capacity is mC. If the switch Sa is carried out to one, the value of input capacitance will serve as 2mC, and if the switch Sa is turned OFF, the value of input capacitance will serve as mC. Therefore, at the time of a differential double end input, by turning OFF the switch Sa, a profit will be 1 time and a profit will be twice by carrying out the switch Sa to one at the time of a single-ended input.

[0163]In the example of drawing 11, the parallel circuit of m capacitor Ca is connected between the inversed input terminal of the operational amplifier 110, and the inverted output terminal. Similarly, the parallel circuit of m capacitor Ca is connected between the non-inversed input terminal of the operational amplifier 110, and the noninverting output terminal. The parallel circuit of 2m piece capacitor Cc is connected to the inversed input terminal of the operational amplifier 110, the 2m piece capacitor Cb is connected to the parallel circuit of capacitor Cc, and the switch Sa is connected to the capacitor Cb in parallel. The parallel circuit of 2m piece capacitor Cc is connected to a non-inversed input terminal, the 2m piece capacitor Cb is connected to the parallel circuit of capacitor Cc, and the switch Sa is connected to the capacitor Cb in parallel. The composition of other portions of the arithmetic amplifier 11a of drawing 11 is the same as the composition of the arithmetic amplifier 11a of drawing 6.

[0164]In this example, the value of feed back capacity is mC. If the switch Sa is carried out to one, the value of input capacitance will serve as 2mC, and if the switch Sa is turned OFF, the value of input capacitance will serve as mC. Therefore, at the time of a differential double end input, by turning OFF the switch Sa, a profit will be 1 time and a profit will be twice by carrying

out the switch Sa to one at the time of a single-ended input.

[0165]In the arithmetic amplifier 11a of drawing 6 - drawing 11, the switch Sa is constituted by the MOS transistor as mentioned above. The diffusion capacitance of a MOS transistor is added to the node to which the switch Sa is connected by that cause, and gate capacitance is added at the time of one of the switch Sa. If capacity is added to the inversed input terminal or non-inversed input terminal of the operational amplifier 110, the working speed of the arithmetic amplifier 11a will fall.

[0166]The switch Sa is connected to the inverted output terminal and noninverting output terminal of the operational amplifier 110 in the example of drawing 6 and drawing 7. Thereby, the working speed of the arithmetic amplifier 11a does not fall. Therefore, the example of drawing 6 and drawing 7 is preferred.

[0167]Since on resistance exists at the time of one of the switch Sa when the switch Sa is connected in parallel with a capacitor, the capacity of a capacitor is thoroughly unseparable.

[0168]In the example of drawing 6, the switch Sa is connected to capacitor Ca in series, and the switch Sa is connected to the inverted output terminal and noninverting output terminal of the operational amplifier 110. Thereby, the capacity of capacitor Ca is thoroughly separable at the time of one of the switch Sa. Therefore, the example of drawing 6 is the most preferred.

[0169]In the example of drawing 9, the switch S1a and S2a are connected to the input side rather than the capacitor Cb. On the contrary, when the capacitor Cb is connected to the input side rather than the switch S1a and S2a, even if the switch S1a and S2a are set as an OFF state, the parasitic capacitance of the capacitor Cb is charged. By that cause, it will be necessary to take parasitic capacitance into consideration, and a profit will vary with dispersion in parasitic capacitance at the time of setting out of a profit. Like the example of drawing 9, by connecting the switch S1a and S2a to an input side rather than the capacitor Cb, when the switch S1a and S2a are set as an OFF state, the capacitor Cb is separated by the switch S1a and S2a with parasitic capacitance. Therefore, in the example of drawing 9, it becomes unnecessary to take the parasitic capacitance of the capacitor Cb into consideration at the time of setting out of a profit, and dispersion in the profit by dispersion in parasitic capacitance is lost.

[0170]The circuit diagram showing the 1st example of the composition of sub A/D converter [in / in drawing 12 / the analog-to-digital circuit 1 of drawing 1] 9a and drawing 13 are the circuit diagrams showing the composition of the comparator used for sub A/D converter 9a of drawing 12.

[0171]Sub A/D converter 9a is provided with the circuit generating reference voltage 92, 93a, and 93b and two or more comparators 90 which generate reference voltage in drawing 12.

[0172]The circuit generating reference voltage 92 consists of two or more resistance R connected in series. The circuit generating reference voltage 93a consists of two or more resistance R connected in series. The circuit generating reference voltage 93b consists of two or more resistance R1 connected in series. Two or more resistance R has equal resistance, and two or more resistance R1 has equal resistance.

[0173]The circuit generating reference voltage 92 is connected between the node N91 which receives the high potential side reference voltage VRT, and the node N92 which receives the low voltage side reference voltage VRB. The circuit generating reference voltage 93a is connected via the switch S24 and S25 between the node N93 which receives the high potential side reference voltage VRT, and the node N94 which receives the low voltage side reference voltage VRB. The circuit generating reference voltage 93b is connected between the node N93 which receives the high potential side reference voltage VRT, and the node N94 which receives the low voltage side reference voltage VRB. The switch S26 is connected between the intermediate node N95 of the circuit generating reference voltage 93a, and the intermediate node N96 of the circuit generating reference voltage 93b.

[0174]Reference voltage which is different at the node during the resistance R of the circuit generating reference voltage 92, respectively is generated. Similarly, reference voltage which is different at the node during the resistance R of the circuit generating reference voltage 93a, respectively is generated. Here, different reference voltage obtained by the circuit generating

reference voltage 92 is called the right side reference voltage $V_{ref}(+)$. Different reference voltage obtained by the circuit generating reference voltage 93a is called the negative side reference voltage $V_{ref}(-)$.

[0175] Middle reference voltage $VRT1 = (VRT - VRB)/2$ which is the middle voltage of the high potential side reference voltage VRT and the low voltage side reference voltage VRB is generated by the intermediate node N96 of the circuit generating reference voltage 93b.

[0176] As shown in drawing 13, each comparator 90 includes the operational amplifier 91, the capacitor C1, C2, and the switches S13–S18. The switch S13 is connected between the inversed input terminal of the operational amplifier 91, and an inversed output terminal, and the switch S14 is connected between the non-inversed input terminal and the noninverting output terminal. The capacitor C1 is connected to the inversed input terminal of the operational amplifier 91, and the capacitor C2 is connected to the non-inversed input terminal. The switch S15 and S16 are connected to the capacitor C1, and the switch S17 and S18 are connected to the capacitor C2. In drawing 12, the switch S13 of each comparator 90 and the graphic display of S14 are omitted.

[0177] The right side analog input voltage $V_{in}(+)$ and the right side reference voltage $V_{ref}(+)$ are given to the capacitor C1 via the switch S15 and S16, respectively. The negative side analog input voltage $V_{in}(-)$ and the negative side reference voltage $V_{ref}(-)$ are given to the capacitor C2 via the switch S17 and S18, respectively.

[0178] In the initial state, the switch S16 and S18 turn off. [the switch S13 S14, S15, and S17] Next, the one [the switch S15 and S17 are turned off and / the switch S16 and S18] after turning off the switch S13 and S14. Since the inversed input terminal and non-inversed input terminal of the operational amplifier 91 are floating when the switch S13 and S14 are turned off, The voltage of an inversed input terminal changes ($V_{in}(+) - V_{ref}(+)$), and the voltage of a non-inversed input terminal changes ($V_{in}(-) - V_{ref}(-)$). As a result, differential analog input voltage ($V_{in}(+) - V_{in}(-)$) and differential reference voltage ($V_{ref}(+) - V_{ref}(-)$) are measured, and right side analog-output-voltage $V_{out}(+)$ and negative side analog-output-voltage $V_{out}(-)$ change according to a comparison result.

[0179] The digital code Dcode can be obtained by encoding the comparison result of two or more comparators 90 of drawing 12 with the encoder 950.

[0180] In sub A/D converter 9a of drawing 12, at the time of a differential double end input, and the switch S26 is turned off. [the switch S24 and S25] Thereby, the negative side reference voltage $V_{ref}(-)$ which changes with circuit generating reference voltage 93a via the switch S18, respectively to the capacitor C2 of each comparator 90 is given. At the time of a single-ended input, the switch S24 and S25 are turned off and the switch S26 is carried out to one. Thereby, middle reference voltage $VRT1$ is given to the capacitor C2 of each comparator 90 by the circuit generating reference voltage 93b via the switch S18.

[0181] Thus, a full-scale range is changed in sub A/D converter 9a.

[0182] The switch S26 may be connected between the intermediate node N95 of the circuit generating reference voltage 93a, and the intermediate node of the circuit generating reference voltage 92, without forming the circuit generating reference voltage 93b.

[0183] The circuit diagram showing the 2nd example of the composition of sub A/D converter [in / in drawing 14 / the analog-to-digital circuit 1 of drawing 1] 9a and drawing 15 are the circuit diagrams showing the composition of the comparator used for sub A/D converter 9a of drawing 14.

[0184] In drawing 14, the switch S26 of drawing 12 is not connected between the intermediate node N95 of the circuit generating reference voltage 93a, and the intermediate node N96 of the circuit generating reference voltage 93b.

[0185] As shown in drawing 15, each comparator 90 includes the operational amplifier 91, the capacitor C1, C2, and the switches S13–S18, and contains the switch S21 and S22 further. One end of the switch S21 is connected to the capacitor C1, and the other end of the switch S21 is opened wide. One end of the switch S22 is connected to the capacitor C2, and the other end is connected to the intermediate node N96 of the reference voltage generating time 93b of drawing 14. The composition of other portions of the comparator 90 of drawing 15 is the same as the composition of the comparator 90 of drawing 13.

[0186]Middle reference voltage VRT1 is given to the capacitor C2 by the reference voltage generating time 93b via the switch S22.

[0187]Operation of the comparator 90 of drawing 15 at the time of a differential double end input is the same as operation of the comparator 90 of drawing 13. At this time, the switch S21 and S22 are always turned off. At the time of a single-ended input, the switch S22 is operated instead of the switch S18. At this time, the switch S21 is always turned off.

[0188]The one [the switch S24 and S25] at the time of a differential double end input in sub A/D converter 9a of drawing 14. At this time, the switch S21 and S22 are always turned OFF. Thereby, the negative side reference voltage Vref (-) which changes with circuit generating reference voltage 93a via the switch S18, respectively to the capacitor C2 of each comparator 90 is given. At the time of a single-ended input, the switch S24 and S25 are turned off and the switch S22 is operated instead of the switch S18. At this time, the switch S21 is always turned off. Thereby, middle reference voltage VRT1 is given to the capacitor C2 of each comparator 90 by the circuit generating reference voltage 93b via the switch S22.

[0189]Thus, a full-scale range is changed in sub A/D converter 9a.

[0190]Although it is not necessary to form the switch S21 in each comparator 90, in order to secure the symmetry of the circuitry of the comparator 90, it is preferred to form the switch S21.

[0191]Drawing 16 is a circuit diagram of sub A/D converter 9b in the 2nd step of circuit 4 in the analog-to-digital circuit 1 of drawing 3. Sub A/D converter 9b of drawing 16 is a full-parallel comparison (flash plate) method sub A/D converter.

[0192]Sub A/D converter 9b comprises the circuit generating reference voltage 94 and 95 and two or more comparators 90 which generate reference voltage. Each of the circuit generating reference voltage 94 and 95 consists of the resistance R2 or 2n resistance R of a piece and, and the resistance R3. The resistance R2 and R3 have resistance n times the resistance of R, respectively. The resistance R2 or 2n resistance R of a piece and, and the resistance R3 are connected between the node N97 which receives high potential side reference voltage VRT2, and the node N98 which receives low voltage side reference voltage VRB2. The switch S28 is connected to the both ends of the resistance R2, and the switch S29 is connected to the both ends of the resistance R3.

[0193]Reference voltage which is different at the node during the resistance R of the circuit generating reference voltage 94, respectively is generated. Similarly, reference voltage which is different at the node during the resistance R of the circuit generating reference voltage 95, respectively is generated. Here, different reference voltage obtained by the circuit generating reference voltage 94 is called the right side reference voltage Vref (+). Different reference voltage obtained by the circuit generating reference voltage 95 is called the negative side reference voltage Vref (-).

[0194]The right side analog input voltage Vin (+) and the right side reference voltage Vref (+) are given to the capacitor C1 of each comparator 90 via the switch S15 and S16, respectively. The negative side analog input voltage Vin (-) and the negative side reference voltage Vref (-) are given to the capacitor C2 of each comparator 90 via the switch S17 and S18, respectively. The composition and operation of the comparator 90 of drawing 16 are the same as the composition of the comparator 90 of drawing 13, and operation.

[0195]Here, the difference of high potential side reference voltage VRT2 and low voltage side reference voltage VRB2 is set as $VIN_{p-p}/8$. When the switch S28 of the circuit generating reference voltage 95 and 96 and S29 are OFF, full-scale ranges are $VIN_{p-p}/16$. If the switch S28 and S29 are made one, a full-scale range will be set to $VIN_{p-p}/8$. Thus, in sub A/D converter 9b, a full-scale range can be changed 1 time and twice.

[0196]Drawing 17 is a circuit diagram of D/A converter 10 in the 2nd step of circuit 4 in the analog-to-digital circuit 1 of drawing 3. D/A converter 10 of drawing 17 is a capacity array method D/A converter.

[0197]D/A converter 10 comprises the switch S51 by the side of right [of the each plurality connected to the circuit generating reference voltage 96 which generates reference voltage, and

array form], S52 and the switch S53 of two or more negative sides, S54, two or more right side capacitors C50, and two or more negative side capacitors C51.

[0198]The circuit generating reference voltage 96 consists of the resistance R4, two or more resistance R, and the resistance R5. The resistance R4 and R5 have the resistance of the half of the resistance of the sum total of two or more resistance R. The resistance R4, two or more resistance R, and the resistance R5 are connected in series between the node N101 which receives high potential side reference voltage VRT3, and the node N102 which receives low voltage side reference voltage VRB3. The switch S30 is connected to the both ends of the resistance R4, and the switch S31 is connected to the both ends of the resistance R5.

[0199]All of the capacitor C50 and C51 have the same capacity value. From one terminal (it is hereafter called an output terminal) N111 of the capacitor C50, the differential positive side output voltage VDA (+) is generated, and the differential negative side output voltage VDA (-) is generated from one terminal (henceforth an output terminal) N112 of the capacitor C51. Each capacitor C50 and the terminal of another side of C51 are called an input terminal.

[0200]One terminal of each switch S51 is connected to the node N103 between the resistance R4 and the resistance R, and the terminal of another side is connected to the input terminal of the capacitor C50. One terminal of each switch S52 is connected to the node N104 between the resistance R5 and the resistance R, and the terminal of another side is connected to the input terminal of the capacitor C50. One terminal of each switch S53 is connected to the node N103 between the resistance R4 and the resistance R, and the terminal of another side is connected to the input terminal of the capacitor C51. One terminal of each switch S54 is connected to the node N104 between the resistance R5 and the resistance R, and the terminal of another side is connected to the input terminal of the capacitor C51.

[0201]According to the output level of the comparator 90 of sub A/D converter 9b of drawing 16, on-off control action of the switch S51, S52, S53, and S54 is carried out. The four switches S51 which receive the output signal of the same comparator 90, S52, S53, and S54 constitute 4 ream switch. For example, when the output of the one comparator 90 is high-level, and the switch S52 and S53 turn off. [the switch S51 of 4 ream switch, and S54] On the contrary, one [the switch S51 of 4 ream switch and S54 turn off, and / the switch S52 and S53] when the output of the one comparator 90 is a low level.

[0202]According to the output level of two or more comparators 90 of sub A/D converter 9b, two or more switches S51, S52, S53, and S54 carry out on-off control action, and the differential positive side output voltage VDA (+) and the differential negative side output voltage VDA (-) are obtained by the output terminal N111 and N112.

[0203]Here, the difference of high potential side reference voltage VRT3 and low voltage side reference voltage VRB3 is set as $VIN_{p-p}/4$. When the switch S30 of the circuit generating reference voltage 96 and S31 are OFF, full-scale ranges are $VIN_{p-p}/8$. If the switch S30 and S31 are made one, a full-scale range will be set to $VIN_{p-p}/4$. Thus, in D/A converter 10b, a full-scale range can be changed 1 time and twice.

[0204]Drawing 18 is a circuit diagram showing the 1st example of the composition of the subtraction amplifier 14a in the analog-to-digital circuit 1 of drawing 3.

[0205]The subtraction amplifier 14a of drawing 18 includes the operational amplifier 130, the capacity value switching circuit 131,132, the capacitor 133,134, and the switches 135-138. A switch is constituted by the MOS (metal oxide semiconductor) transistor, for example.

[0206]The capacity value switching circuit 131 is connected as feed back capacity between the inversed input terminal of the operational amplifier 130, and an inverted output terminal, and the capacity value switching circuit 132 is connected as feed back capacity between the non-inversed input terminal and the noninverting output terminal. The capacitor 133 is connected to the inversed input terminal of the operational amplifier 130 as input capacitance, and the capacitor 134 is connected to the non-inversed input terminal as input capacitance.

[0207]The differential positive side output voltage VDA (+) outputted from the right side analog output voltage Vo (+) and D/A converter 10b which are outputted is given to the capacitor 133 via the switch 135,136, respectively from the arithmetic amplifier 11 of drawing 3. The differential

positive side output voltage VDA (−) outputted from the negative side analog output voltage Vo (−) and D/A converter 10b which are outputted is given to the capacitor 134 via the switch 137,138, respectively from the arithmetic amplifier 11. The inversed input terminal, the inverted output terminal, non-inversed input terminal, and noninverting output terminal of the operational amplifier 130 are grounded via the switch 139,140,141,142, respectively.

[0208]Operation of the subtraction amplifier 14a of drawing 18 is the same as operation of the arithmetic amplifier 11a of drawing 4. The right side analog input voltage Vin (+) and the negative side analog input voltage Vin (−) which are given in the circuit 4 of the next step are obtained from the inverted output terminal and noninverting output terminal of the operational amplifier 130.

[0209]Here, the profit of the subtraction amplifier 14a can be changed by changing the capacity value of the capacity value switching circuit 131,132.

[0210]Drawing 19 is a circuit diagram showing the 2nd example of the composition of the subtraction amplifier 14a in the analog-to-digital circuit 1 of drawing 3.

[0211]The subtraction amplifier 14a of drawing 19 includes the operational amplifier 130, the capacitor 139,140, the capacity value switching circuit 141,142, and the switches 135–140.

[0212]The capacitor 139 is connected as feed back capacity between the inversed input terminal of the operational amplifier 130, and an inverted output terminal, and the capacitor 140 is connected as feed back capacity between the non-inversed input terminal and the noninverting output terminal. The capacity value switching circuit 141 is connected to the inversed input terminal of the operational amplifier 130 as input capacitance, and the capacity value switching circuit 142 is connected to the non-inversed input terminal as input capacitance.

[0213]The differential positive side output voltage VDA (+) outputted from the right side analog output voltage Vo (+) and D/A converter 10b which are outputted is given to the capacity value switching circuit 141 via the switch 135,136, respectively from the arithmetic amplifier 11 of drawing 3. The differential positive side output voltage VDA (−) outputted from the negative side analog output voltage Vo (−) and D/A converter 10b which are outputted is given to the capacity value switching circuit 142 via the switch 137,138, respectively from the arithmetic amplifier 11. The inversed input terminal, the inverted output terminal, non-inversed input terminal, and noninverting output terminal of the operational amplifier 130 are grounded via the switch 139,140,141,142, respectively.

[0214]Operation of the subtraction amplifier 14a of drawing 19 is the same as operation of the arithmetic amplifier 11a of drawing 5. The right side analog input voltage Vin (+) and the negative side analog input voltage Vin (−) which are given in the circuit 4 of the next step are obtained from the inverted output terminal and noninverting output terminal of the operational amplifier 130.

[0215]Here, the profit of the subtraction amplifier 14a can be changed by changing the capacity value of the capacity value switching circuit 141,142.

[0216]The switch Sa of the above-mentioned embodiment, S1a, S2a, S24, S25, S26, S28, S29, S30, and S31 are formed, for example of an MOS (metal oxide semiconductor) field effect transistor.

[0217]According to the above-mentioned embodiment, the switch Sa, S1a, S2a, S24, S25, S26, S28, S29, S30, and S31 are used as a switch part of a switching means. In this case, the switch Sa, S1a, S2a, S24, S25, S26, S28, S29, S30, and S31 can be changed to one or OFF at the time of manufacture or use. The switch part of a switching means is not limited to a switch. For example, the fuse which can be blown out with laser may be used as a switch part, and the mask switch part for patterning of top layer metal may be used as a switch part.

[0218]Drawing 20 is a circuit diagram showing other examples of a switch part. In the example of drawing 20, the fuse Fa is used instead of the switch Sa of the arithmetic amplifier 11a of drawing 6. The fuse Fa can consist of polysilicon, for example, and can be blown out with laser. At the time of manufacture, the profit of the arithmetic amplifier 11a can be changed by whether laser is used and the fuse Fa is blown out.

[0219]Drawing 21 and drawing 22 are the figures showing the example of further others of a switch part, show a top view to the upper part and show a sectional view to the lower part.

[0220]In the capacity formation section C500, the electrode 501,502 of the capacitor is formed of lower layer metal LM1 and LM2. The electrode 507,508 is formed of lower layer metal LM1. With the top layer metal UM, the electrode 512,513 is formed with a prescribed interval, and the electrode 514,515 is formed with the prescribed interval. The electrode 501 is connected to the electrode 512 via the metal in the through hole 503, and the electrode 502 is connected to the electrode 514 via the metal in the through hole 504. The electrode 507 is connected to the electrode 512 via the metal in the through hole 505, and the electrode 508 is connected to the electrode 515 via the metal in the through hole 506.

[0221]For example, 507 is connected to the inversed input terminal of the operational amplifier 110 of drawing 6, and the electrode 508 is connected to the inverted output terminal of the operational amplifier 110 of drawing 6.

[0222]The capacity formation section C500 is formed of the electrode 501,502, and mask switch part municipal solid waste is formed between the electrodes 512,513 and of between the electrodes 514,515, respectively. The capacity formation block C500 is equivalent to capacitor Ca of drawing 6, for example.

[0223]At the time of manufacture, between the electrodes 512,513 and between the electrodes 514,515 can be changed to a connected state and a cut off state by changing the pattern of the mask arranged on mask switch part municipal solid waste.

[0224]As shown in drawing 21, between the electrodes 512,513 and between the electrodes 514,515 are connectable by using the mask that the metal layer 510,511 is formed with the top layer metal UM between the electrodes 512,513 and between the electrodes 514,515.

[0225]As shown in drawing 22, between the electrodes 512,513 and between the electrodes 514,515 can be intercepted by using the mask that a metal layer is not formed with the top layer metal UM between the electrodes 512,513 and between the electrodes 514,515.

[0226]In the example of drawing 21 and drawing 22, the capacity formation section C500 is thoroughly separable from an operational amplifier by providing a mask switch part in the terminal of both capacity formation sections C500, respectively.

[0227]In the circuit of the stages with an arbitrary analog-to-digital circuit in which this invention is not limited to the above-mentioned embodiment, At least one of the D/A converters which have an arithmetic amplifier which has a switchable profit, a subtraction amplifier which has a switchable profit, a sub A/D converter which has a switchable full-scale range, and a switchable full-scale range may be used.

[Translation done.]

* NOTICES *

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TECHNICAL FIELD

[Field of the Invention]This invention relates to the analog-to-digital circuit which has multi stage pipeline (step flash plate) composition.

[Translation done.]

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PRIOR ART

[Description of the Prior Art]In recent years, the demand of the analog-to-digital circuits for video signal processing (A/D converter) is large with progress of the digital processing art of a video signal. Since fast conversion operation was required of the analog-to-digital circuit for video signal processing, 2 step flash plate (parallel two steps) method was used widely conventionally.

[0003]However, since conversion precision sufficient by 2 step flash plate method was no longer acquired with increase of the conversion number of bits, the analog-to-digital circuit which has multi stage pipeline (step flash plate) composition was developed.

[0004]Drawing 23 is a block diagram showing the conventional analog-to-digital circuit indicated by JP,11-88172,A. The analog-to-digital circuit 100 of drawing 23 has 10-bit four-step pipeline constitution.

[0005]In drawing 23, the analog-to-digital circuit 100 comprises the circuits 3-6, two or more latch circuitry 7, and the output circuit 8 of the 2 or 1st step - the 4th step of sample hold circuit.

[0006]The 1st (first rank) step - the 3rd step of circuits 3, 4, and 5 are provided with sub A/D converter 9, D/A converter 10, the arithmetic amplifier 11, the subtractor circuit 12, and the arithmetic amplifier 13. The subtractor circuit 12 and the arithmetic amplifier 13 constitute the subtraction amplifier 14. The profit of the arithmetic amplifier 11 in the 1st step of circuit 3 is 1, and the profit of the arithmetic amplifiers 11 and 13 in the arithmetic amplifier 13 in the 1st step of circuit 3, the 2nd step, and the 3rd step of circuit 4 and 5 is 2. The 4th (final stage) step of circuit 6 is provided only with sub A/D converter 9.

[0007]4 bit configurations and the 2-4th step of circuits 4-6 of the 1st step of circuit 3 are 2 bit configurations, respectively. Similarly in the 1-3rd step of circuits 3-5, the number of bits (bit configuration) of sub A/D converter 9 and D/A converter 10 is set up.

[Translation done.]

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- 3.In the drawings, any words are not translated.

EFFECT OF THE INVENTION

[The means for solving a technical problem and an effect of the invention] (1) The analog-to-digital circuit concerning the 1st invention invention of the 1st, Have the multi stage pipeline constitution which consists of two or more steps of circuits, and the circuit of each stage except the circuit of a final stage, The analog-digital converter which changes the inputted analog signal into a digital signal, The digital-to-analog converter which changes into an analog signal the digital signal outputted from an analog-digital converter, Have the 1st arithmetic amplifier that amplifies the difference of the analog signal inputted and the analog signal outputted from a digital-to-analog converter, and the circuit of a final stage, The analog-digital converter which changes the inputted analog signal into a digital signal is included, The analog-digital converter which has a switching means from which at least one step of circuit except the circuit of a final stage changes a full-scale range to two or more steps, At least one of the 1st arithmetic amplifiers that have a switching means which changes the digital-to-analog converter and profit which have a switching means which changes a full-scale range to two or more steps to two or more steps is included, And/or, the circuit of a final stage contains the analog-digital converter which has a switching means which changes a full-scale range to two or more steps. [0045]In an analog-to-digital circuit concerning this invention, An analog-digital converter which has a switching means from which at least one step of circuit except a circuit of a final stage changes a full-scale range to two or more steps, At least one of the 1st arithmetic amplifiers that have a switching means which changes a digital-to-analog converter and a profit which have a switching means which changes a full-scale range to two or more steps, and to change to two or more steps is included, And/or, since a circuit of a final stage contains an analog-digital converter which has a switching means which changes a full-scale range to two or more steps, At least one of a full-scale range of an analog-to-digital circuit, a full-scale range of a digital-to-analog converter, and profits of the 1st arithmetic amplifier can be changed.

[0046]Redesign of circuitry becomes unnecessary even if a voltage range of an analog input signal is changed by that cause by changing a differential double end input method into a single-ended input method. Redesign of circuitry becomes unnecessary, when changing a voltage range of an analog input signal of a single-ended input, or also when changing a voltage range of an analog input signal of a differential double end input.

[0047]Therefore, an input method between change of a voltage range of an analog input signal or a differential double end input, and a single-ended input can be changed easily, without redesigning circuitry.

[0048]As a result, while being able to attain shortening of a development cycle of an analog-to-digital circuit, low power consumption can be easily performed by optimizing optimization of a voltage range.

[0049](2) An analog-to-digital circuit concerning the 2nd invention invention of the 2nd, In composition of an analog-to-digital circuit concerning the 1st invention, a circuit of each stage except a circuit of a final stage, The 2nd arithmetic amplifier of at least one step of circuit except a circuit of a final stage has a switching means which changes a profit to two or more steps, including further the 2nd arithmetic amplifier that amplifies an inputted analog signal and is given to the 1st arithmetic amplifier.

[0050]In this case, by changing a profit of the 2nd arithmetic amplifier of at least one step of circuit to two or more steps, It becomes possible to change an input method between change of a voltage range of an analog input signal or a differential double end input, and a single-ended input easily, without redesigning circuitry.

[0051](3) In composition of an analog-to-digital circuit which an analog-to-digital circuit concerning the 3rd invention invention of the 3rd requires for the 1st or 2nd invention, the 1st arithmetic amplifier of at least one step of circuit except a circuit of a final stage has a switching means which changes a profit to two or more steps.

[0052]In this case, by changing a profit of the 1st arithmetic amplifier of at least one step of circuit to two or more steps, It becomes possible to change an input method between change of a voltage range of an analog input signal or a differential double end input, and a single-ended input easily, without redesigning circuitry.

[0053](4) An analog-to-digital circuit concerning the 4th invention invention of the 4th, In composition of an analog-to-digital circuit concerning the 1st – the 3rd one of inventions, an analog-digital converter of at least one step of circuit has a switching means which changes a full-scale range to two or more steps.

[0054]In this case, a full-scale range of an analog-digital converter of at least one step of circuit to two or more steps by switchable *****. It becomes possible to change an input method between change of a voltage range of an analog input signal or a differential double end input, and a single-ended input easily, without redesigning circuitry.

[0055](5) An analog-to-digital circuit concerning the 5th invention invention of the 5th, In composition of an analog-to-digital circuit concerning the 1st – the 4th one of inventions, a digital-to-analog converter of at least one step of circuit except a circuit of a final stage has a switching means which changes a full-scale range to two or more steps.

[0056]In this case, by changing a full-scale range of a digital-to-analog converter of at least one step of circuit to two or more steps, It becomes possible to change an input method between change of a voltage range of an analog input signal or a differential double end input, and a single-ended input easily, without redesigning circuitry.

[0057](6) An analog-to-digital circuit concerning the 6th invention invention of the 6th, In composition of an analog-to-digital circuit concerning the 2nd invention, the 2nd arithmetic amplifier of at least one step of circuit, It has input capacitance, feedback capacity, and an operational amplifier, an inputted analog signal is amplified on a profit which becomes settled with a value of input capacitance, and a value of feedback capacity, and a switching means contains a variable region which sets either [at least] a value of input capacitance, or a value of feedback capacity as variable.

[0058]In this case, an inputted analog signal is amplified on a profit which becomes settled with a value of input capacitance, and a value of feedback capacity. Therefore, a profit of the 2nd arithmetic amplifier can be easily changed by changing either [at least] a value of input capacitance of an operational amplifier, or a value of feedback capacity.

[0059](7) In composition of an analog-to-digital circuit which requires an analog-to-digital circuit concerning invention the 7th invention of the 7th for the 6th invention, a variable region contains a switch part changed to a state or the state where it connected too hastily where a part of input capacitance or feedback capacity was separated.

[0060]In this case, input capacitance or feedback capacity of an operational amplifier can be changed by changing to a state or the state where it connected too hastily where a part of input capacitance or feedback capacity was separated by switch part. Thereby, a profit of the 2nd arithmetic amplifier can be changed easily.

[0061](8) An analog-to-digital circuit concerning the 8th invention invention of the 8th, In composition of an analog-to-digital circuit concerning the 3rd invention, the 1st arithmetic amplifier of at least one step of circuit, It has input capacitance, feedback capacity, and an operational amplifier, an inputted analog signal is amplified on a profit which becomes settled with a value of input capacitance, and a value of feedback capacity, and a switching means contains a variable region which sets either [at least] a value of input capacitance, or a value of feedback capacity as variable.

[0062]In this case, an inputted analog signal is amplified on a profit which becomes settled with a value of input capacitance, and a value of feedback capacity. Therefore, a profit of the 1st arithmetic amplifier can be easily changed by changing either [at least] a value of input capacitance of an operational amplifier, or a value of feedback capacity.

[0063](9) In composition of an analog-to-digital circuit which requires an analog-to-digital circuit concerning invention the 9th invention of the 9th for the 8th invention, a variable region contains a switch part changed to a state or the state where it connected too hastily where a part of input capacitance or feedback capacity was separated.

[0064]In this case, input capacitance or feedback capacity of an operational amplifier can be changed from changing to a state or the state where it connected too hastily where a part of input capacitance or feedback capacity was separated by switch part. Thereby, a profit of the 1st arithmetic amplifier can be changed easily.

[0065](10) An analog-to-digital circuit concerning the 10th invention invention of the 10th, In composition of an analog-to-digital circuit concerning the 9th invention, a switch part is connected to the 2nd capacity in series or in parallel including the 1st and 2nd capacity by which feedback capacity was provided in parallel or in series between an input terminal of an operational amplifier, and an output terminal.

[0066]If a switch part is made into a connected state, the 1st and 2nd capacity will be connected in parallel or in series between an input terminal of an operational amplifier, and an output terminal. Thereby, feedback capacity increases or decreases. If a switch part is made into a cut off state, only the 1st capacity will be connected between an input terminal of an operational amplifier, and an output terminal. Thereby, feedback capacity decreases or increases.

[0067](11) A switch part is connected to an output terminal of an operational amplifier in composition of an analog-to-digital circuit which requires an analog-to-digital circuit concerning invention the 11th invention of the 11th for the 10th invention.

[0068]When the 2nd capacity is connected to an output side rather than a switch part, even if a switch part is set as a cut off state, parasitic capacitance of the 2nd capacity is charged. By that cause, it will be necessary to take parasitic capacitance into consideration, and a profit will vary with dispersion in parasitic capacitance at the time of setting out of a profit. Here, by connecting a switch part to an output side rather than the 2nd capacity, when a switch part is set as a cut off state, the 2nd capacity is separated from an output terminal by switch part with parasitic capacitance. Therefore, it becomes unnecessary to take parasitic capacitance of the 2nd capacity into consideration at the time of setting out of a profit, and dispersion in a profit by dispersion in parasitic capacitance is lost.

[0069](12) In composition of an analog-to-digital circuit which requires an analog-to-digital circuit concerning invention the 12th invention of the 12th for the 9th invention, input capacitance is provided in an input terminal of an operational amplifier in parallel or in series.

[0070]If a switch part is made into a connected state, the 1st and 2nd capacity will be connected to an input terminal of an operational amplifier in parallel or in series. Thereby, input capacitance increases or decreases. Only the 1st capacity will be connected to an input terminal of an operational amplifier if a switch part is made into a cut off state. Thereby, input capacitance decreases or increases.

[0071](13) A switch part is connected to an input side of the 2nd capacity in composition of an analog-to-digital circuit which requires an analog-to-digital circuit concerning invention the 13th invention of the 13th for the 12th invention.

[0072]When the 2nd capacity is connected to an input side rather than a switch part, even if a switch part is set as a cut off state, parasitic capacitance of the 2nd capacity is charged. By that cause, it will be necessary to take parasitic capacitance into consideration, and a profit will vary with dispersion in parasitic capacitance at the time of setting out of a profit. Here, by connecting a switch part to an input side rather than the 2nd capacity, when a switch part is set as a cut off state, it is separated from a node in which the 2nd capacity receives an input signal by a switch part with parasitic capacitance. Therefore, it becomes unnecessary to take parasitic capacitance of the 2nd capacity into consideration at the time of setting out of a profit, and

dispersion in a profit by dispersion in parasitic capacitance is lost.

[0073](14) An analog-to-digital circuit concerning the 14th invention invention of the 14th, In composition of an analog-to-digital circuit concerning the 4th invention, an analog-digital converter of at least one step of circuit, A switching means contains a variable region which sets as variable two or more reference voltage generated by circuit generating reference voltage including circuit generating reference voltage which generates two or more reference voltage, and two or more comparators compared with an analog signal into which two or more reference voltage generated by circuit generating reference voltage was inputted.

[0074]In this case, a voltage range of reference voltage can be changed by changing reference voltage generated by circuit generating reference voltage. Thereby, a full-scale range of an analog-digital converter can be changed easily.

[0075](15) An analog-to-digital circuit concerning the 15th invention invention of the 15th, In composition of an analog-to-digital circuit concerning the 5th invention, a digital-to-analog converter of at least one step of circuit except a circuit of a final stage, Circuit generating reference voltage which generates reference voltage, and two or more capacity connected to a common terminal, Two or more switches which give reference voltage which was connected between circuit generating reference voltage and two or more capacity, and was generated by circuit generating reference voltage according to a digital signal inputted to two or more capacity, respectively are included, A switching means contains a variable region which sets reference voltage generated by circuit generating reference voltage as variable.

[0076]In this case, a voltage range of reference voltage can be changed by changing reference voltage generated by circuit generating reference voltage. Thereby, a full-scale range of a digital-to-analog converter can be changed easily.

[0077]

[Embodiment of the Invention](1) The 1st embodiment drawing 1 is a block diagram showing the composition of the pipeline type analog-to-digital circuit in a 1st embodiment of this invention. The analog-to-digital circuit of drawing 1 has 10-bit four-step pipeline constitution.

[0078]In drawing 1, the analog-to-digital circuit 1 comprises the circuits 3-6, two or more latch circuitry 7, and the output circuit 8 of the 2 or 1st step - the 4th step of sample hold circuit.

[0079]The 1st (first rank) step of circuit 3 is provided with the arithmetic amplifier 11a, the subtractor circuit 12, and the arithmetic amplifier 13 which have sub A/D converter 9a which has a switchable full-scale range, D/A converter 10, and a switchable profit. The subtractor circuit 12 and the arithmetic amplifier 13 constitute the subtraction amplifier 14. The 2nd step and the 3rd step of circuits 4 and 5 are provided with sub A/D converter 9, D/A converter 10, the arithmetic amplifier 11, the subtractor circuit 12, and the arithmetic amplifier 13. The subtractor circuit 12 and the arithmetic amplifier 13 constitute the subtraction amplifier 14. The 4th (final stage) step of circuit 6 is provided only with sub A/D converter 9.

[0080]That the pipeline type analog-to-digital circuit 1 of drawing 1 differs from the conventional analog-to-digital circuit 100 of drawing 20, It is the point that the arithmetic amplifier 11a which has sub A/D converter 9a and the switchable profit which have a switchable full-scale range is used for the 1st step of circuit 3.

[0081]Here, the full-scale range of sub A/D converter 9 in the 1st step of circuit 3, It changes to voltage range VIN_{p-p} equal to it when the voltage range of an analog input signal is VIN_{p-p} , and when the voltage ranges of an analog input signal are $VIN_{p-p}/2$, it changes to voltage range $VIN_{p-p}/2$. [equal to it] The profit of the arithmetic amplifier 11a in the 1st step of circuit 3 is changed 1 time, when the voltage range of an analog input signal is VIN_{p-p} , and when the voltage ranges of an analog input signal are $VIN_{p-p}/2$, it is changed twice.

[0082]The full-scale range of D/A converter 10 in the 1st step - the 3rd step of circuit 3-5 is fixed, and the full-scale range of sub A/D converter 9 in the 2nd step - the 4th step of circuit 4-6 is being fixed. The profit of the arithmetic amplifiers 11 and 13 in the arithmetic amplifier 13 in the 1st step of circuit 3, the 2nd step, and the 3rd step of circuit 3 and 4 is 2.

[0083]4 bit configurations and the 2-4th step of circuits 4-6 of the 1st step of circuit 3 are 2 bit

configurations, respectively. Similarly in the 1-3rd step of circuits 3-5, the number of bits (bit configuration) of sub A/D converters 9 and 9a and D/A converter 10 is set up.

[0084] Operation of the analog-to-digital circuit 1 of drawing 1 in case the voltage range of an analog input signal is VIN_{p-p} , and the voltage range of each part are the same as that of the analog-to-digital circuit 100 of drawing 20.

[0085] Here, operation of the analog-to-digital circuit 1 of drawing 1 in case the voltage ranges of an analog input signal are $VIN_{p-p}/2$, and the output voltage range of each part are explained.

[0086] The sample hold circuit 2 samples the analog input signal Vin , and carries out fixed time maintenance. The analog input signal Vin outputted from the sample hold circuit 2 is transmitted to the 1st step of circuit 3.

[0087] In the 1st step of circuit 3, sub A/D converter 9a performs an analog to digital to the analog input signal Vin of voltage range $VIN_{p-p}/2$. The full-scale range of sub A/D converter 9a at this time is changed to $VIN_{p-p}/2$ as mentioned above.

[0088] Top 4-bit digital output ($2^9, 2^8, 2^7, 2^6$) which is an A/D conversion result of sub A/D converter 9a is transmitted to the output circuit 8 via the four latch circuitry 7 while it is transmitted to D/A converter 10. D/A converter 10 changes into an analog signal top 4-bit digital output which is an A/D conversion result of sub A/D converter 9a.

[0089] Since the full-scale range of D/A converter 10 is being fixed to VIN_{p-p} , the normal output voltage range of D/A converter 10 is expressed like a following formula.

[0090]

(The 1st step of resolution-1) \times (full-scale range of D/A converter 10) / (the 1st step of resolution)

$= (2^4 - 1) \times (VIN_{p-p}) / 2^4 = 15VIN_{p-p}/16$ one side and the arithmetic amplifier 11a sample the analog input signal Vin , and amplify and hold it. As mentioned above, since a profit is changed twice when the voltage ranges of an analog input signal are $VIN_{p-p}/2$, the output voltage range of the arithmetic amplifier 11a is expressed like a following formula.

[0091]

(Voltage range of the analog input signal Vin) \times (profit of the arithmetic amplifier 11a)

$= (VIN_{p-p}/2) \times 2 = VIN_{p-p}$ subtraction amplifier 14 subtracts and amplifies the analog input signal Vin and the D/A conversion result of D/A converter 10 which were outputted from the arithmetic amplifier 11a. The output of the subtraction amplifier 14 is transmitted to the 2nd step of circuit 4.

[0092] The output voltage range of the 1st step of subtraction amplifier 14 is expressed like a following formula.

(Output voltage range of the arithmetic amplifier 11a) \times (- (normal output voltage range of D/A converter 10)) (profit of the subtraction amplifier 14)

$= (VIN_{p-p}) \times (- (15VIN_{p-p}/16))$ In the $\times 2 = VIN_{p-p}/82$ step circuit 4, sub A/D converter 9 performs an A/D conversion to the output of the subtraction amplifier 14 of the 1st step of circuit 3. The A/D conversion result of sub A/D converter 9 is transmitted to the output circuit 8 via the three latch circuitry 7 while it is transmitted to D/A converter 10. Thereby, a 2-bit digital output ($2^5, 2^4$) is obtained at least for Nakagami from the 2nd step of circuit 4.

[0093] On the other hand, the arithmetic amplifier 11 amplifies the output of the subtraction amplifier 14 of the 1st step of circuit 3. The subtraction amplifier 14 subtracts and amplifies the output of the arithmetic amplifier 11, and the D/A conversion result of D/A converter 10. The output of the subtraction amplifier 14 is transmitted to the 3rd step of circuit 5.

[0094] In the 3rd step of circuit 5, the same operation as the 2nd step of circuit 4 is performed to the output of the subtraction amplifier 14 of the 2nd step of circuit 4. Thereby, a 2-bit digital output ($2^3, 2^2$) is obtained at least for Nakashita from the 3rd step of circuit 5.

[0095] In the 4th step of circuit 6, sub A/D converter 9 performs an A/D conversion to the output of the subtraction amplifier 14 of the 3rd step of circuit 5, and the digital output ($2^1, 2^0$)

of 2 bits of low ranks is obtained.

[0096]The digital output of the 1st step – the 4th step of circuits 3–6 arrives at the output circuit 8 simultaneously through each latch circuitry 7. That is, each latch circuitry 7 is formed in order to take the synchronization of the digital output of each circuits 3–6.

[0097]The output circuit 8 carries out the after [a digital compensation process] parallel output of the 10-bit digital output Dout of the analog input signal Vin, when required.

[0098]As mentioned above, when the voltage ranges of an analog input signal are $VIN_{p-p}/2$. By changing the full-scale range of the profit of the arithmetic amplifier 11a of the 1st step of circuit 3, and sub A/D converter 9a of the 1st step of circuit 3, The voltage range of the output signal given in the 2nd step of circuit 5 is set to $VIN_{p-p}/8$ from the subtraction amplifier 14 of the 1st step of circuit 3 like the case where the voltage range of an analog input signal is VIN_{p-p} . Thereby, although the voltage range of the analog input signal Vin became half, the digital output same before the voltage range of an analog input signal becomes half is obtained.

[0099]Therefore, the analog-to-digital circuit corresponding to change of the voltage range of an analog input signal can be provided, without changing a circuit design.

[0100]According to this embodiment, the analog-to-digital circuit of a differential double end input method can be changed into the analog-to-digital circuit of a single-ended input method, without changing circuitry.

[0101]Drawing 2 (a) and (b) is a figure showing setting out in the case of changing the analog-to-digital circuit 1 of drawing 1 to a differential double end input method and a single-ended input method, respectively.

[0102]As shown in drawing 2 (a), at the time of a differential double end input, the profit of the arithmetic amplifier 11a is changed 1 time, and the full-scale range of sub A/D converter 9a is changed to $2VIN_{p-p}$. In this example, the right side analog input voltage Vin of the analog input signal Vin of a differential double end input (+) changes in 1.0V to 2.0V, and the negative side analog input voltage Vin (-) changes from 2.0V in 1.0V. The voltage range of the analog input signal Vin becomes like a following formula.

[0103]The maximum of $2VIN_{p-p} = \{Vin(+)-Vin(-)\} - \text{minimum} = 2.0 [V]$ of $\{Vin(+)-Vin(-)\}$

In this case, the right side reference voltage Vref of sub A/D converter 9a (+) changes in 1.0V to 2.0V, and the negative side reference voltage Vref (-) changes from 2.0V in 1.0V.

[0104]As shown in drawing 2 (b), at the time of a single-ended input, the profit of the arithmetic amplifier 11a is changed twice, and the full-scale range of sub A/D converter 9a is changed to VIN_{p-p} . The right side analog input voltage Vin of the analog input signal Vin of the single-ended input in this example (+) changes in 1.0V to 2.0V, and that of the negative side analog input voltage Vin (-) is constant 1.5V. The voltage range of the analog input signal Vin becomes like a following formula.

[0105]The maximum of $VIN_{p-p} = \{Vin(+)-Vin(-)\} - \text{minimum} = 1.0 [V]$ of $\{Vin(+)-Vin(-)\}$

In this case, the right side reference voltage Vref of sub A/D converter 9a (+) changes in 1.0V to 2.0V, and its negative side reference voltage Vref (-) is constant 1.5V.

[0106]Thus, in the analog-to-digital circuit 1 of drawing 1, even if the voltage range of an analog input signal is set to one half by changing a differential double end input method into a single-ended input method, redesign of circuitry becomes unnecessary.

[0107]Redesign of circuitry becomes unnecessary, when changing the voltage range of the analog input signal of a single-ended input into one half, and also when changing the voltage range of the analog input signal of a differential double end input into one half.

[0108]Thus, in the same LSI (large scale integration circuit), the voltage range of the output of an analog input signal and an arithmetic amplifier, the output of a D/A conversion circuit, and the output of a subtraction amplifier can be changed programmably. As a result, while being able to attain shortening of a development cycle, it is also possible to perform low power consumption.

[0109](2) The 2nd embodiment drawing 3 is a block diagram showing the composition of the pipeline type analog-to-digital circuit in a 2nd embodiment of this invention. The analog-to-

digital circuit 1 of drawing 3 also has 10-bit four-step pipeline constitution.

[0110]In drawing 3, the analog-to-digital circuit 1 comprises the circuits 3-6, two or more latch circuitry 7, and the output circuit 8 of the 2 or 1st step - the 4th step of sample hold circuit.

[0111]4 bit configurations and the 2-4th step of circuits 4-6 of the 1st step of circuit 3 are 2 bit configurations, respectively. Similarly in the 1-3rd step of circuits 3-5, the number of bits (bit configuration) of sub A/D converters 9 and 9b and D/A converters 10 and 10b is set up.

[0112]The 1st (first rank) step of circuit 3 is provided with the arithmetic amplifier 13a which has sub A/D converter 9, D/A converter 10, the arithmetic amplifier 11, the subtractor circuit 12, and a switchable profit. The subtractor circuit 12 and the arithmetic amplifier 13a constitute the subtraction amplifier 14a.

[0113]The 2nd step and the 3rd step of circuits 4 and 5 are provided with sub A/D converter 9b which has a switchable full-scale range, D/A converter 10b which has a switchable full-scale range, the arithmetic amplifier 11, the subtractor circuit 12, and the arithmetic amplifier 13. The subtractor circuit 12 and the arithmetic amplifier 13 constitute the subtraction amplifier 14. The 4th (final stage) step of circuit 6 is provided only with sub A/D converter 9b which has a switchable full-scale range.

[0114]Here, the 2nd step - the 4th step of sub A/D converter 9b shall have the 2nd step - the 4th step of A/D converter 9 of drawing 20 twice the accuracy of sub. Redesign of the analog-to-digital circuit 1 at the time of using for the 2nd step - the 4th step hereafter sub A/D converter 9b which has twice as many accuracy as this is explained.

[0115]It is switchable 1 time and twice in the profit of the subtraction amplifier 14a in the 1st step of circuit 3. It is switchable to $VIN_{p-p}/8$, and $VIN_{p-p}/16$ in the full-scale range of sub A/D converter 9b in the 2nd step - the 4th step of circuit 4-6. It is switchable to $VIN_{p-p}/4$, and $VIN_{p-p}/8$ in the full-scale range of D/A converter 10b in the 2nd step and the 3rd step of circuit 4 and 5.

[0116]Here, the profit of the subtraction amplifier 14a in the 1st step of circuit 3 is changed 1 time. The full-scale range of sub A/D converter 9b in the 2nd step - the 4th step of circuit 4-6 is changed to $VIN_{p-p}/16$, and the full-scale range of D/A converter 10b in the 2nd step and the 3rd step of circuit 4 and 5 is changed to $VIN_{p-p}/8$. The full-scale range of sub A/D converter 9 in the 1st step of circuit 3 is VIN_{p-p} . The profit of the arithmetic amplifiers 11 and 13 in the 2nd step and the 3rd step of circuit 3 and 4 is 2.

[0117]Here, operation of the analog-to-digital circuit 1 of drawing 1 in case the voltage range of an analog input signal is VIN_{p-p} , and the output voltage range of each part are explained.

[0118]The sample hold circuit 2 samples the analog input signal Vin , and carries out fixed time maintenance. The analog input signal Vin outputted from the sample hold circuit 2 is transmitted to the 1st step of circuit 3.

[0119]In the 1st step of circuit 3, sub A/D converter 9 performs an analog to digital to the analog input signal Vin of voltage range VIN_{p-p} . The full-scale range of sub A/D converter 9 at this time is VIN_{p-p} .

[0120]Top 4-bit digital output ($2^9, 2^8, 2^7, 2^6$) which is an A/D conversion result of sub A/D converter 9 is transmitted to the output circuit 8 via the four latch circuitry 7 while it is transmitted to D/A converter 10. D/A converter 10 changes into an analog signal top 4-bit digital output which is an A/D conversion result of sub A/D converter 9.

[0121]Since the full-scale range of D/A converter 10 is being fixed, the normal output voltage range of D/A converter 10 is expressed like a following formula.

[0122]

(The 1st step of resolution-1) x (full-scale range of D/A converter 10) / (the 1st step of resolution)

$= (2^4 - 1) \times (VIN_{p-p}) / 2^4 = 15VIN_{p-p}/16$ one side and the arithmetic amplifier 11 sample the analog input signal Vin , and amplify and hold it. Since the profit of the arithmetic amplifier 11 is 1

time, the output voltage range of the arithmetic amplifier 11 is expressed like a following formula.

[0123]

(Voltage range of the analog input signal V_{in}) x (profit of the arithmetic amplifier 11)
 = The $V_{IN_{p-p}} \times 1 = V_{IN_{p-p}}$ subtraction amplifier 14a subtracts and amplifies the analog input signal V_{in} and the D/A conversion result of D/A converter 10 which were outputted from the arithmetic amplifier 11. The output of the subtraction amplifier 14a is transmitted to the 2nd step of circuit 4.

[0124] Since the profit of the 1st step of subtraction amplifier 14a is changed to 1, the output voltage range of the 1st step of subtraction amplifier 14a is expressed like a following formula.

[0125]

(Output voltage range of the arithmetic amplifier 11) x (– (normal output voltage range of D/A converter 10)) (profit of the subtraction amplifier 14a)
 = $(V_{IN_{p-p}}) (- (15V_{IN_{p-p}}/16))$ In the $x1 = V_{IN_{p-p}}/162$ step circuit 4, sub A/D converter 9b performs an A/D conversion to the output of the subtraction amplifier 14a of the 1st step of circuit 3. The A/D conversion result of sub A/D converter 9b is transmitted to the output circuit 8 via the three latch circuitry 7 while it is transmitted to D/A converter 10b.

[0126] In this case, since sub A/D converter 9b has A/D converter 9 of drawing 20 twice the accuracy of sub, A 2-bit digital output ($2^5, 2^4$) is obtained at least for Nakagami from the 2nd step of circuit 4 by full-scale range $V_{IN_{p-p}}/16$ of the half of sub A/D converter 9 of drawing 20.

[0127] At least Nakagami whose D/A converter 10b is an A/D conversion result of sub A/D converter 9b changes a 2-bit digital output into an analog signal.

[0128] Since the full-scale range of D/A converter 10b is changed to $V_{IN_{p-p}}/8$ of the half of D/A converter 10 of drawing 20, the normal output voltage range of D/A converter 10b is expressed like a following formula.

[0129]

(The 2nd step of resolution–1) x (full-scale range of D/A converter 10b)
 /(the 2nd step of resolution)
 = $(2^2-1) \times (V_{IN_{p-p}}/8) / 2^2 = 3V_{IN_{p-p}}/32$ one side and the arithmetic amplifier 11 amplify the output of the subtraction amplifier 14a of the 1st step of circuit 3. As mentioned above, since the profit of the subtraction amplifier 14a of the 1st step of circuit 3 is changed to 1, the output voltage range of the arithmetic amplifier 11a is expressed like a following formula.

[0130]

(Output voltage range of the 1st step of subtraction amplifier 14a) x (profit of the arithmetic amplifier 11)
 = $(V_{IN_{p-p}}/16)$ The $x2 = V_{IN_{p-p}}/8$ subtraction amplifier 14 subtracts and amplifies the output of the arithmetic amplifier 11, and the D/A conversion result of D/A converter 10b. The output of the subtraction amplifier 14 is transmitted to the 3rd step of circuit 5.

[0131] The output voltage range of the 2nd step of subtraction amplifier 14 is expressed like a following formula.

(Output voltage range of the arithmetic amplifier 11) x (– (normal output voltage range of D/A converter 10b)) (profit of the subtraction amplifier 14)
 = $(V_{IN_{p-p}}/8) (- (3V_{IN_{p-p}}/32))$ In the $x2 = V_{IN_{p-p}}/163$ step circuit 5, the same operation as the 2nd step of circuit 4 is performed to the output of the subtraction amplifier 14 of the 2nd step of circuit 4. In this case, since sub A/D converter 9b has A/D converter 9 of drawing 20 twice the accuracy of sub, A 2-bit digital output ($2^3, 2^2$) is obtained at least for Nakashita from the 3rd step of circuit 5 by full-scale range $V_{IN_{p-p}}/16$ of the half of sub A/D converter 9 of drawing 20.
 The output voltage range of each part is the same as that of the 2nd step of circuit 4.

[0132] In the 4th step of circuit 6, sub A/D converter 9b performs an A/D conversion to the output of the subtraction amplifier 14 of the 3rd step of circuit 5. In this case, since sub A/D

converter 9b has A/D converter 9 of drawing 20 twice the accuracy of sub, The digital output ($2^1, 2^0$) of 2 bits of low ranks is obtained from the 4th step of circuit 6 by full-scale range $V_{IN_{p-}}/16$ of the half of sub A/D converter 9 of drawing 20.

[0133]The digital output of the 1st step – the 4th step of circuits 3–6 arrives at the output circuit 8 simultaneously through each latch circuitry 7. That is, each latch circuitry 7 is formed in order to take the synchronization of the digital output of each circuits 3–6.

[0134]The output circuit 8 carries out the after [a digital compensation process] parallel output of the 10-bit digital output Dout of the analog input signal Vin, when required.

[0135]As mentioned above, in the analog-to-digital circuit 1 of drawing 3. Although the voltage range of each part of the circuits 4–6 after the 2nd step became half [of the analog-to-digital circuit 100 of drawing 20] by using sub A/D converter 9b which has twice as many accuracy as this, the digital output same before a voltage range becomes half is obtained.

[0136]In this case, the alternating current component of current which flows through the circuits 3–6 of each stage decreases by optimizing a voltage range to sub A/D converter 9b which has twice as many accuracy as this, and setting it as a half. Thereby, the consumed electric current can provide the analog-to-digital circuit by which reduction was carried out by optimizing a voltage range, without changing a circuit design.

[0137](3) Circuitry drawing 4 of each part is a circuit diagram showing the 1st example of the composition of the arithmetic amplifier 11a in the analog-to-digital circuit 1 of drawing 1.

[0138]The arithmetic amplifier 11a of drawing 4 includes the operational amplifier 110, the capacity value switching circuit 111,112, the capacitor 113,114, and the switches 115–122. The switches 115–122 are constituted by the MOS (metal oxide semiconductor) transistor, for example.

[0139]The capacity value switching circuit 111 is connected as feed back capacity between the inversed input terminal of the operational amplifier 110, and an inversed output terminal, and the capacity value switching circuit 112 is connected as feed back capacity between the non-inversed input terminal and the noninverting output terminal. The capacitor 113 is connected to the inversed input terminal of the operational amplifier 110 as input capacitance, and the capacitor 114 is connected to the non-inversed input terminal as input capacitance.

[0140]The right side analog input voltage Vin (+) and middle reference voltage VRT1 are given to the capacitor 113 via the switch 115,116, respectively. The negative side analog input voltage Vin (–) and middle reference voltage VRT1 are given to the capacitor 114 via the switch 117,118, respectively. The inversed input terminal, the inversed output terminal, non-inversed input terminal, and noninverting output terminal of the operational amplifier 110 are grounded via the switch 119,120,121,122, respectively.

[0141]If capacity value of the capacitor 113,114 is set to CA, respectively and capacity value of the capacity value switching circuit 111,112 is set to CB here, respectively, The right side analog output voltage Vo of the inversed output terminal of the operational amplifier 110 (+) and the negative side analog output voltage Vo of a noninverting output terminal (–) become like a following formula.

[0142]

$$V_o(+)= (V_{in}(+)-VRT1) \text{ and } (CA/CB)$$

$$V_o(-)= (V_{in}(-)-VRT1) \text{ and } (CA/CB)$$

$$\Delta V_o = V_o(+)-V_o(-)$$

$$= (V_{in}(+)-V_{in}(-)) -(CA/CB)$$

Therefore, the profit of the arithmetic amplifier 11a can be changed by changing the capacity value CB of the capacity value switching circuit 111,112.

[0143]Drawing 5 is a circuit diagram showing the 2nd example of the composition of the arithmetic amplifier 11a in the analog-to-digital circuit 1 of drawing 1.

[0144]The arithmetic amplifier 11a of drawing 5 includes the operational amplifier 110, the capacitor 123,124, the capacity value switching circuit 125,126, and the switches 115–122.

[0145]The capacitor 123 is connected as feed back capacity between the inversed input terminal of the operational amplifier 110, and an inversed output terminal, and the capacitor 124 is

connected as feed back capacity between the non-inversed input terminal and the noninverting output terminal. The capacity value switching circuit 125 is connected to the inversed input terminal of the operational amplifier 110 as input capacitance, and the capacity value switching circuit 126 is connected to the non-inversed input terminal as input capacitance.

[0146]The right side analog input voltage $V_{in}(+)$ and middle reference voltage V_{RT1} are given to the capacity value switching circuit 125 via the switch 115,116, respectively. The negative side analog input voltage $V_{in}(-)$ and middle reference voltage V_{RT1} are given to the capacity value switching circuit 126 via the switch 117,118, respectively. The inversed input terminal, the inverted output terminal, non-inversed input terminal, and noninverting output terminal of the operational amplifier 110 are grounded via the switch 119,120,121,122, respectively.

[0147]If capacity value of the capacity value switching circuit 125,126 is set to CC, respectively and capacity value of the capacitor 123,124 is set to CD here, respectively, The right side analog output voltage V_o of the inverted output terminal of the operational amplifier 110 (+) and the negative side analog output voltage V_o of a noninverting output terminal (-) become like a following formula.

[0148]

$$V_o(+) = (V_{in}(+) - V_{RT1}) \text{ and } (CC/CD)$$

$$V_o(-) = (V_{in}(-) - V_{RT1}) \text{ and } (CC/CD)$$

$$\Delta V_o = V_o(+) - V_o(-)$$

$$= (V_{in}(+) - V_{in}(-)) - (CC/CD)$$

Therefore, the profit of the arithmetic amplifier 11a can be changed by changing capacity value CC of the capacity value switching circuit 125,126.

[0149]Drawing 6 - drawing 11 are the circuit diagrams showing the 1st - the 6th example of the concrete circuitry of the arithmetic amplifier 11a.

[0150]In drawing 6 - drawing 11, each of the capacitors C_a , C_b , and C_c shall have the equal capacity value C. Let m be arbitrary positive integers.

[0151]In the example of drawing 6, the parallel circuit and the switch S_a of m capacitor C_a are connected in series between the inversed input terminal of the operational amplifier 110, and an inverted output terminal, and the parallel circuit of m capacitor C_a is connected. Here, m is arbitrary positive integers. Similarly, the parallel circuit and the switch S_a of m capacitor C_a are connected in series between the non-inversed input terminal of the operational amplifier 110, and a noninverting output terminal, and the parallel circuit of m capacitor C_a is connected. The 2m piece capacitor C_b is connected to the inversed input terminal of the operational amplifier 110, and the 2m piece capacitor C_b is connected to the non-inversed input terminal.

[0152]The right side analog input voltage $V_{in}(+)$ is given to the 2m piece capacitor C_b by the side of an inversed input terminal via the switch S_1 , respectively. The negative side analog input voltage $V_{in}(-)$ is given to the capacitor C_b by the side of a non-inversed input terminal via the switch S_1 , respectively. The high potential side reference voltage V_{RT} is given to the m capacitors C_b by the side of an inversed input terminal, and the m capacitors C_b by the side of a non-inversed input terminal via the switch S_2 , respectively, The low voltage side reference voltage V_{RB} is given to the m capacitors C_b by the side of a non-inversed input terminal, and the m capacitors C_b by the side of a non-inversed input terminal via the switch S_2 , respectively.

[0153]In this example, the values of input capacitance are 2mC. If the switch S_a is carried out to one, the value of feed back capacity will serve as 2mC, and if the switch S_a is turned OFF, the value of feed back capacity will serve as mC. Therefore, at the time of a differential double end input, by changing the switch S_a to one, a profit will be 1 time and a profit will be twice by changing the switch S_a to OFF at the time of a single-ended input.

[0154]In the example of drawing 7, the parallel circuit of 2m piece capacitor C_a and the parallel circuit of 2m piece capacitor C_c are connected in series between the inversed input terminal of the operational amplifier 110, and an inverted output terminal, and the switch S_a is connected in parallel with capacitor C_c . Similarly, the parallel circuit of 2m piece capacitor C_a and the parallel circuit of 2m piece capacitor C_c are connected in series between the non-inversed input terminal of the operational amplifier 110, and a noninverting output terminal, and the switch S_a is

connected in parallel with capacitor C_c . The composition of other portions of the arithmetic amplifier 11a of drawing 7 is the same as that of the arithmetic amplifier 11a of drawing 6.

[0155]In this example, the values of input capacitance are $2mC$. If the switch S_a is carried out to one, the value of feed back capacity will serve as $2mC$, and if the switch S_a is turned OFF, the value of feed back capacity will serve as mC . Therefore, at the time of a differential double end input, by changing the switch S_a to one, a profit will be 1 time and a profit will be twice by changing the switch S_a to OFF at the time of a single-ended input.

[0156]In the example of drawing 8, the parallel circuit of $2m$ piece capacitor C_a and the parallel circuit of $2m$ piece capacitor C_c are connected in series between the inversed input terminal of the operational amplifier 110, and an inverted output terminal, and the switch S_a is connected in parallel with capacitor C_a . Similarly, the parallel circuit of $2m$ piece capacitor C_a and the parallel circuit of $2m$ piece capacitor C_c are connected in series between the non-inversed input terminal of the operational amplifier 110, and a noninverting output terminal, and the switch S_a is connected in parallel with capacitor C_a . The composition of other portions of the arithmetic amplifier 11a of drawing 8 is the same as that of the arithmetic amplifier 11a of drawing 6.

[0157]In this example, the values of input capacitance are $2mC$. If the switch S_a is carried out to one, the value of feed back capacity will serve as $2mC$, and if the switch S_a is turned OFF, the value of feed back capacity will serve as mC . Therefore, at the time of a differential double end input, by changing the switch S_a to one, a profit will be 1 time and a profit will be twice by changing the switch S_a to OFF at the time of a single-ended input.

[0158]In the example of drawing 9, the parallel circuit of m capacitor C_a is connected between the inversed input terminal of the operational amplifier 110, and the inverted output terminal. Similarly, the parallel circuit of m capacitor C_a is connected between the non-inversed input terminal of the operational amplifier 110, and the noninverting output terminal. The $2m$ piece capacitor C_b is connected to the inversed input terminal of the operational amplifier 110, and the $2m$ piece capacitor C_b is connected to the non-inversed input terminal.

[0159]The right side analog input voltage $V_{in}(+)$ is given to the $2m$ piece capacitor C_b by the side of an inversed input terminal via the switch S_1 and S_{1a} , respectively. The negative side analog input voltage $V_{in}(-)$ is given to the capacitor C_b by the side of a non-inversed input terminal via the switch S_1 and S_{1a} , respectively. The high potential side reference voltage V_{RT} is given to the m capacitors C_b by the side of an inversed input terminal, and the m capacitors C_b by the side of a non-inversed input terminal via the switch S_2 and S_{2a} , respectively. The low voltage side reference voltage V_{RB} is given to the m capacitors C_b by the side of a non-inversed input terminal, and the m capacitors C_b by the side of a non-inversed input terminal via the switch S_2 and S_{2a} , respectively.

[0160]In this example, the value of feed back capacity is mC . If the switch S_{1a} and S_{2a} are made one, the value of input capacitance will serve as $2mC$, and if the switch S_{1a} and S_{2a} are turned OFF, the value of input capacitance will serve as mC . Therefore, at the time of a differential double end input, by always turning OFF the switch S_{1a} and S_{2a} , a profit will be 1 time and a profit will be twice by carrying out switching operation of the switch S_{1a} and the S_{2a} like the switch S_1 and S_2 at the time of a single-ended input.

[0161]In the example of drawing 10, the parallel circuit of m capacitor C_a is connected between the inversed input terminal of the operational amplifier 110, and the inverted output terminal. Similarly, the parallel circuit of m capacitor C_a is connected between the non-inversed input terminal of the operational amplifier 110, and the noninverting output terminal. The parallel circuit of $2m$ piece capacitor C_c is connected to the inversed input terminal of the operational amplifier 110, the $2m$ piece capacitor C_b is connected to the parallel circuit of capacitor C_c , and the switch S_a is connected in parallel with capacitor C_c . The parallel circuit of $2m$ piece capacitor C_c is connected to a non-inversed input terminal, the $2m$ piece capacitor C_b is connected to the parallel circuit of capacitor C_c , and the switch S_a is connected in parallel with capacitor C_c . The composition of other portions of the arithmetic amplifier 11a of drawing 10 is the same as that of the arithmetic amplifier 11a of drawing 6.

[0162]In this example, the value of feed back capacity is mC . If the switch S_a is carried out to one, the value of input capacitance will serve as $2mC$, and if the switch S_a is turned OFF, the

value of input capacitance will serve as mC . Therefore, at the time of a differential double end input, by turning OFF the switch S_a , a profit will be 1 time and a profit will be twice by carrying out the switch S_a to one at the time of a single-ended input.

[0163]In the example of drawing 11, the parallel circuit of m capacitor C_a is connected between the inversed input terminal of the operational amplifier 110, and the inverted output terminal. Similarly, the parallel circuit of m capacitor C_a is connected between the non-inversed input terminal of the operational amplifier 110, and the noninverting output terminal. The parallel circuit of $2m$ piece capacitor C_c is connected to the inversed input terminal of the operational amplifier 110, the $2m$ piece capacitor C_b is connected to the parallel circuit of capacitor C_c , and the switch S_a is connected to the capacitor C_b in parallel. The parallel circuit of $2m$ piece capacitor C_c is connected to a non-inversed input terminal, the $2m$ piece capacitor C_b is connected to the parallel circuit of capacitor C_c , and the switch S_a is connected to the capacitor C_b in parallel. The composition of other portions of the arithmetic amplifier 11a of drawing 11 is the same as the composition of the arithmetic amplifier 11a of drawing 6.

[0164]In this example, the value of feed back capacity is mC . If the switch S_a is carried out to one, the value of input capacitance will serve as $2mC$, and if the switch S_a is turned OFF, the value of input capacitance will serve as mC . Therefore, at the time of a differential double end input, by turning OFF the switch S_a , a profit will be 1 time and a profit will be twice by carrying out the switch S_a to one at the time of a single-ended input.

[0165]In the arithmetic amplifier 11a of drawing 6 - drawing 11, the switch S_a is constituted by the MOS transistor as mentioned above. The diffusion capacitance of a MOS transistor is added to the node to which the switch S_a is connected by that cause, and gate capacitance is added at the time of one of the switch S_a . If capacity is added to the inversed input terminal or non-inversed input terminal of the operational amplifier 110, the working speed of the arithmetic amplifier 11a will fall.

[0166]The switch S_a is connected to the inverted output terminal and noninverting output terminal of the operational amplifier 110 in the example of drawing 6 and drawing 7. Thereby, the working speed of the arithmetic amplifier 11a does not fall. Therefore, the example of drawing 6 and drawing 7 is preferred.

[0167]Since on resistance exists at the time of one of the switch S_a when the switch S_a is connected in parallel with a capacitor, the capacity of a capacitor is thoroughly unseparable.

[0168]In the example of drawing 6, the switch S_a is connected to capacitor C_a in series, and the switch S_a is connected to the inverted output terminal and noninverting output terminal of the operational amplifier 110. Thereby, the capacity of capacitor C_a is thoroughly separable at the time of one of the switch S_a . Therefore, the example of drawing 6 is the most preferred.

[0169]In the example of drawing 9, the switch S_{1a} and S_{2a} are connected to the input side rather than the capacitor C_b . On the contrary, when the capacitor C_b is connected to the input side rather than the switch S_{1a} and S_{2a} , even if the switch S_{1a} and S_{2a} are set as an OFF state, the parasitic capacitance of the capacitor C_b is charged. By that cause, it will be necessary to take parasitic capacitance into consideration, and a profit will vary with dispersion in parasitic capacitance at the time of setting out of a profit. Like the example of drawing 9, by connecting the switch S_{1a} and S_{2a} to an input side rather than the capacitor C_b , when the switch S_{1a} and S_{2a} are set as an OFF state, the capacitor C_b is separated by the switch S_{1a} and S_{2a} with parasitic capacitance. Therefore, in the example of drawing 9, it becomes unnecessary to take the parasitic capacitance of the capacitor C_b into consideration at the time of setting out of a profit, and dispersion in the profit by dispersion in parasitic capacitance is lost.

[0170]The circuit diagram showing the 1st example of the composition of sub A/D converter [in / in drawing 12 / the analog-to-digital circuit 1 of drawing 1] 9a and drawing 13 are the circuit diagrams showing the composition of the comparator used for sub A/D converter 9a of drawing 12.

[0171]Sub A/D converter 9a is provided with the circuit generating reference voltage 92, 93a, and 93b and two or more comparators 90 which generate reference voltage in drawing 12.

[0172]The circuit generating reference voltage 92 consists of two or more resistance R

connected in series. The circuit generating reference voltage 93a consists of two or more resistance R connected in series. The circuit generating reference voltage 93b consists of two or more resistance R1 connected in series. Two or more resistance R has equal resistance, and two or more resistance R1 has equal resistance.

[0173]The circuit generating reference voltage 92 is connected between the node N91 which receives the high potential side reference voltage VRT, and the node N92 which receives the low voltage side reference voltage VRB. The circuit generating reference voltage 93a is connected via the switch S24 and S25 between the node N93 which receives the high potential side reference voltage VRT, and the node N94 which receives the low voltage side reference voltage VRB. The circuit generating reference voltage 93b is connected between the node N93 which receives the high potential side reference voltage VRT, and the node N94 which receives the low voltage side reference voltage VRB. The switch S26 is connected between the intermediate node N95 of the circuit generating reference voltage 93a, and the intermediate node N96 of the circuit generating reference voltage 93b.

[0174]Reference voltage which is different at the node during the resistance R of the circuit generating reference voltage 92, respectively is generated. Similarly, reference voltage which is different at the node during the resistance R of the circuit generating reference voltage 93a, respectively is generated. Here, different reference voltage obtained by the circuit generating reference voltage 92 is called the right side reference voltage Vref (+). Different reference voltage obtained by the circuit generating reference voltage 93a is called the negative side reference voltage Vref (-).

[0175]Middle reference voltage VRT1 ($= (VRT - VRB) / 2$) which is the middle voltage of the high potential side reference voltage VRT and the low voltage side reference voltage VRB is generated by the intermediate node N96 of the circuit generating reference voltage 93b.

[0176]As shown in drawing 13, each comparator 90 includes the operational amplifier 91, the capacitor C1, C2, and the switches S13-S18. The switch S13 is connected between the inversed input terminal of the operational amplifier 91, and an inverted output terminal, and the switch S14 is connected between the non-inversed input terminal and the noninverting output terminal. The capacitor C1 is connected to the inversed input terminal of the operational amplifier 91, and the capacitor C2 is connected to the non-inversed input terminal. The switch S15 and S16 are connected to the capacitor C1, and the switch S17 and S18 are connected to the capacitor C2. In drawing 12, the switch S13 of each comparator 90 and the graphic display of S14 are omitted.

[0177]The right side analog input voltage Vin (+) and the right side reference voltage Vref (+) are given to the capacitor C1 via the switch S15 and S16, respectively. The negative side analog input voltage Vin (-) and the negative side reference voltage Vref (-) are given to the capacitor C2 via the switch S17 and S18, respectively.

[0178]In the initial state, and the switch S16 and S18 turn off. [the switch S13 S14, S15, and S17] Next, the one [the switch S15 and S17 are turned off and / the switch S16 and S18] after turning off the switch S13 and S14. Since the inversed input terminal and non-inversed input terminal of the operational amplifier 91 are floating when the switch S13 and S14 are turned off, The voltage of an inversed input terminal changes ($Vin(+) - Vref(+)$), and the voltage of a non-inversed input terminal changes ($Vin(-) - Vref(-)$). As a result, differential analog input voltage ($Vin(+) - Vin(-)$) and differential reference voltage ($Vref(+) - Vref(-)$) are measured, and right side analog-output-voltage Vout (+) and negative side analog-output-voltage Vout (-) change according to a comparison result.

[0179]The digital code Dcode can be obtained by encoding the comparison result of two or more comparators 90 of drawing 12 with the encoder 950.

[0180]In sub A/D converter 9a of drawing 12, at the time of a differential double end input, and the switch S26 is turned off. [the switch S24 and S25] Thereby, the negative side reference voltage Vref (-) which changes with circuit generating reference voltage 93a via the switch S18, respectively to the capacitor C2 of each comparator 90 is given. At the time of a single-ended input, the switch S24 and S25 are turned off and the switch S26 is carried out to one. Thereby, middle reference voltage VRT1 is given to the capacitor C2 of each comparator 90 by the circuit generating reference voltage 93b via the switch S18.

[0181] Thus, a full-scale range is changed in sub A/D converter 9a.

[0182] The switch S26 may be connected between the intermediate node N95 of the circuit generating reference voltage 93a, and the intermediate node of the circuit generating reference voltage 92, without forming the circuit generating reference voltage 93b.

[0183] The circuit diagram showing the 2nd example of the composition of sub A/D converter [in / in drawing 14 / the analog-to-digital circuit 1 of drawing 1] 9a and drawing 15 are the circuit diagrams showing the composition of the comparator used for sub A/D converter 9a of drawing 14.

[0184] In drawing 14, the switch S26 of drawing 12 is not connected between the intermediate node N95 of the circuit generating reference voltage 93a, and the intermediate node N96 of the circuit generating reference voltage 93b.

[0185] As shown in drawing 15, each comparator 90 includes the operational amplifier 91, the capacitor C1, C2, and the switches S13-S18, and contains the switch S21 and S22 further. One end of the switch S21 is connected to the capacitor C1, and the other end of the switch S21 is opened wide. One end of the switch S22 is connected to the capacitor C2, and the other end is connected to the intermediate node N96 of the reference voltage generating time 93b of drawing 14. The composition of other portions of the comparator 90 of drawing 15 is the same as the composition of the comparator 90 of drawing 13.

[0186] Middle reference voltage VRT1 is given to the capacitor C2 by the reference voltage generating time 93b via the switch S22.

[0187] Operation of the comparator 90 of drawing 15 at the time of a differential double end input is the same as operation of the comparator 90 of drawing 13. At this time, the switch S21 and S22 are always turned off. At the time of a single-ended input, the switch S22 is operated instead of the switch S18. At this time, the switch S21 is always turned off.

[0188] The one [the switch S24 and S25] at the time of a differential double end input in sub A/D converter 9a of drawing 14. At this time, the switch S21 and S22 are always turned OFF. Thereby, the negative side reference voltage Vref (-) which changes with circuit generating reference voltage 93a via the switch S18, respectively to the capacitor C2 of each comparator 90 is given. At the time of a single-ended input, the switch S24 and S25 are turned off and the switch S22 is operated instead of the switch S18. At this time, the switch S21 is always turned off. Thereby, middle reference voltage VRT1 is given to the capacitor C2 of each comparator 90 by the circuit generating reference voltage 93b via the switch S22.

[0189] Thus, a full-scale range is changed in sub A/D converter 9a.

[0190] Although it is not necessary to form the switch S21 in each comparator 90, in order to secure the symmetry of the circuitry of the comparator 90, it is preferred to form the switch S21.

[0191] Drawing 16 is a circuit diagram of sub A/D converter 9b in the 2nd step of circuit 4 in the analog-to-digital circuit 1 of drawing 3. Sub A/D converter 9b of drawing 16 is a full-parallel comparison (flash plate) method sub A/D converter.

[0192] Sub A/D converter 9b comprises the circuit generating reference voltage 94 and 95 and two or more comparators 90 which generate reference voltage. Each of the circuit generating reference voltage 94 and 95 consists of the resistance R2 or 2n resistance R of a piece and, and the resistance R3. The resistance R2 and R3 have resistance n times the resistance of R, respectively. The resistance R2 or 2n resistance R of a piece and, and the resistance R3 are connected between the node N97 which receives high potential side reference voltage VRT2, and the node N98 which receives low voltage side reference voltage VRB2. The switch S28 is connected to the both ends of the resistance R2, and the switch S29 is connected to the both ends of the resistance R3.

[0193] Reference voltage which is different at the node during the resistance R of the circuit generating reference voltage 94, respectively is generated. Similarly, reference voltage which is different at the node during the resistance R of the circuit generating reference voltage 95, respectively is generated. Here, different reference voltage obtained by the circuit generating reference voltage 94 is called the right side reference voltage Vref (+). Different reference voltage obtained by the circuit generating reference voltage 95 is called the negative side

reference voltage Vref (-).

[0194]The right side analog input voltage Vin (+) and the right side reference voltage Vref (+) are given to the capacitor C1 of each comparator 90 via the switch S15 and S16, respectively. The negative side analog input voltage Vin (-) and the negative side reference voltage Vref (-) are given to the capacitor C2 of each comparator 90 via the switch S17 and S18, respectively. The composition and operation of the comparator 90 of drawing 16 are the same as the composition of the comparator 90 of drawing 13, and operation.

[0195]Here, the difference of high potential side reference voltage VRT2 and low voltage side reference voltage VRB2 is set as $VIN_{p-p}/8$. When the switch S28 of the circuit generating reference voltage 95 and 96 and S29 are OFF, full-scale ranges are $VIN_{p-p}/16$. If the switch S28 and S29 are made one, a full-scale range will be set to $VIN_{p-p}/8$. Thus, in sub A/D converter 9b, a full-scale range can be changed 1 time and twice.

[0196]Drawing 17 is a circuit diagram of D/A converter 10 in the 2nd step of circuit 4 in the analog-to-digital circuit 1 of drawing 3. D/A converter 10 of drawing 17 is a capacity array method D/A converter.

[0197]D/A converter 10 comprises the switch S51 by the side of right [of the each plurality connected to the circuit generating reference voltage 96 which generates reference voltage, and array form], S52 and the switch S53 of two or more negative sides, S54, two or more right side capacitors C50, and two or more negative side capacitors C51.

[0198]The circuit generating reference voltage 96 consists of the resistance R4, two or more resistance R, and the resistance R5. The resistance R4 and R5 have the resistance of the half of the resistance of the sum total of two or more resistance R. The resistance R4, two or more resistance R, and the resistance R5 are connected in series between the node N101 which receives high potential side reference voltage VRT3, and the node N102 which receives low voltage side reference voltage VRB3. The switch S30 is connected to the both ends of the resistance R4, and the switch S31 is connected to the both ends of the resistance R5.

[0199]All of the capacitor C50 and C51 have the same capacity value. From one terminal (it is hereafter called an output terminal) N111 of the capacitor C50, the differential positive side output voltage VDA (+) is generated, and the differential negative side output voltage VDA (-) is generated from one terminal (henceforth an output terminal) N112 of the capacitor C51. Each capacitor C50 and the terminal of another side of C51 are called an input terminal.

[0200]One terminal of each switch S51 is connected to the node N103 between the resistance R4 and the resistance R, and the terminal of another side is connected to the input terminal of the capacitor C50. One terminal of each switch S52 is connected to the node N104 between the resistance R5 and the resistance R, and the terminal of another side is connected to the input terminal of the capacitor C50. One terminal of each switch S53 is connected to the node N103 between the resistance R4 and the resistance R, and the terminal of another side is connected to the input terminal of the capacitor C51. One terminal of each switch S54 is connected to the node N104 between the resistance R5 and the resistance R, and the terminal of another side is connected to the input terminal of the capacitor C51.

[0201]According to the output level of the comparator 90 of sub A/D converter 9b of drawing 16, on-off control action of the switch S51, S52, S53, and S54 is carried out. The four switches S51 which receive the output signal of the same comparator 90, S52, S53, and S54 constitute 4 ream switch. For example, when the output of the one comparator 90 is high-level, and the switch S52 and S53 turn off. [the switch S51 of 4 ream switch, and S54] On the contrary, one [the switch S51 of 4 ream switch and S54 turn off, and / the switch S52 and S53] when the output of the one comparator 90 is a low level.

[0202]According to the output level of two or more comparators 90 of sub A/D converter 9b, two or more switches S51, S52, S53, and S54 carry out on-off control action, and the differential positive side output voltage VDA (+) and the differential negative side output voltage VDA (-) are obtained by the output terminal N111 and N112.

[0203]Here, the difference of high potential side reference voltage VRT3 and low voltage side

reference voltage VRB3 is set as $VIN_{p-p}/4$. When the switch S30 of the circuit generating reference voltage 96 and S31 are OFF, full-scale ranges are $VIN_{p-p}/8$. If the switch S30 and S31 are made one, a full-scale range will be set to $VIN_{p-p}/4$. Thus, in D/A converter 10b, a full-scale range can be changed 1 time and twice.

[0204] Drawing 18 is a circuit diagram showing the 1st example of the composition of the subtraction amplifier 14a in the analog-to-digital circuit 1 of drawing 3.

[0205] The subtraction amplifier 14a of drawing 18 includes the operational amplifier 130, the capacity value switching circuit 131, 132, the capacitor 133, 134, and the switches 135–138. A switch is constituted by the MOS (metal oxide semiconductor) transistor, for example.

[0206] The capacity value switching circuit 131 is connected as feed back capacity between the inversed input terminal of the operational amplifier 130, and an inverted output terminal, and the capacity value switching circuit 132 is connected as feed back capacity between the non-inversed input terminal and the noninverting output terminal. The capacitor 133 is connected to the inversed input terminal of the operational amplifier 130 as input capacitance, and the capacitor 134 is connected to the non-inversed input terminal as input capacitance.

[0207] The differential positive side output voltage VDA (+) outputted from the right side analog output voltage Vo (+) and D/A converter 10b which are outputted is given to the capacitor 133 via the switch 135, 136, respectively from the arithmetic amplifier 11 of drawing 3. The differential positive side output voltage VDA (–) outputted from the negative side analog output voltage Vo (–) and D/A converter 10b which are outputted is given to the capacitor 134 via the switch 137, 138, respectively from the arithmetic amplifier 11. The inversed input terminal, the inverted output terminal, non-inversed input terminal, and noninverting output terminal of the operational amplifier 130 are grounded via the switch 139, 140, 141, 142, respectively.

[0208] Operation of the subtraction amplifier 14a of drawing 18 is the same as operation of the arithmetic amplifier 11a of drawing 4. The right side analog input voltage Vin (+) and the negative side analog input voltage Vin (–) which are given in the circuit 4 of the next step are obtained from the inverted output terminal and noninverting output terminal of the operational amplifier 130.

[0209] Here, the profit of the subtraction amplifier 14a can be changed by changing the capacity value of the capacity value switching circuit 131, 132.

[0210] Drawing 19 is a circuit diagram showing the 2nd example of the composition of the subtraction amplifier 14a in the analog-to-digital circuit 1 of drawing 3.

[0211] The subtraction amplifier 14a of drawing 19 includes the operational amplifier 130, the capacitor 139, 140, the capacity value switching circuit 141, 142, and the switches 135–140.

[0212] The capacitor 139 is connected as feed back capacity between the inversed input terminal of the operational amplifier 130, and an inverted output terminal, and the capacitor 140 is connected as feed back capacity between the non-inversed input terminal and the noninverting output terminal. The capacity value switching circuit 141 is connected to the inversed input terminal of the operational amplifier 130 as input capacitance, and the capacity value switching circuit 142 is connected to the non-inversed input terminal as input capacitance.

[0213] The differential positive side output voltage VDA (+) outputted from the right side analog output voltage Vo (+) and D/A converter 10b which are outputted is given to the capacity value switching circuit 141 via the switch 135, 136, respectively from the arithmetic amplifier 11 of drawing 3. The differential positive side output voltage VDA (–) outputted from the negative side analog output voltage Vo (–) and D/A converter 10b which are outputted is given to the capacity value switching circuit 142 via the switch 137, 138, respectively from the arithmetic amplifier 11. The inversed input terminal, the inverted output terminal, non-inversed input terminal, and noninverting output terminal of the operational amplifier 130 are grounded via the switch 139, 140, 141, 142, respectively.

[0214] Operation of the subtraction amplifier 14a of drawing 19 is the same as operation of the arithmetic amplifier 11a of drawing 5. The right side analog input voltage Vin (+) and the negative side analog input voltage Vin (–) which are given in the circuit 4 of the next step are obtained from the inverted output terminal and noninverting output terminal of the operational amplifier

130.

[0215]Here, the profit of the subtraction amplifier 14a can be changed by changing the capacity value of the capacity value switching circuit 141,142.

[0216]The switch Sa of the above-mentioned embodiment, S1a, S2a, S24, S25, S26, S28, S29, S30, and S31 are formed, for example of an MOS (metal oxide semiconductor) field effect transistor.

[0217]According to the above-mentioned embodiment, the switch Sa, S1a, S2a, S24, S25, S26, S28, S29, S30, and S31 are used as a switch part of a switching means. In this case, the switch Sa, S1a, S2a, S24, S25, S26, S28, S29, S30, and S31 can be changed to one or OFF at the time of manufacture or use. The switch part of a switching means is not limited to a switch. For example, the fuse which can be blown out with laser may be used as a switch part, and the mask switch part for patterning of top layer metal may be used as a switch part.

[0218]Drawing 20 is a circuit diagram showing other examples of a switch part. In the example of drawing 20, the fuse Fa is used instead of the switch Sa of the arithmetic amplifier 11a of drawing 6. The fuse Fa can consist of polysilicon, for example, and can be blown out with laser. At the time of manufacture, the profit of the arithmetic amplifier 11a can be changed by whether laser is used and the fuse Fa is blown out.

[0219]Drawing 21 and drawing 22 are the figures showing the example of further others of a switch part, show a top view to the upper part and show a sectional view to the lower part.

[0220]In the capacity formation section C500, the electrode 501,502 of the capacitor is formed of lower layer metal LM1 and LM2. The electrode 507,508 is formed of lower layer metal LM1. With the top layer metal UM, the electrode 512,513 is formed with a prescribed interval, and the electrode 514,515 is formed with the prescribed interval. The electrode 501 is connected to the electrode 512 via the metal in the through hole 503, and the electrode 502 is connected to the electrode 514 via the metal in the through hole 504. The electrode 507 is connected to the electrode 512 via the metal in the through hole 505, and the electrode 508 is connected to the electrode 515 via the metal in the through hole 506.

[0221]For example, 507 is connected to the inversed input terminal of the operational amplifier 110 of drawing 6, and the electrode 508 is connected to the inverted output terminal of the operational amplifier 110 of drawing 6.

[0222]The capacity formation section C500 is formed of the electrode 501,502, and mask switch part municipal solid waste is formed between the electrodes 512,513 and of between the electrodes 514,515, respectively. The capacity formation block C500 is equivalent to capacitor Ca of drawing 6, for example.

[0223]At the time of manufacture, between the electrodes 512,513 and between the electrodes 514,515 can be changed to a connected state and a cut off state by changing the pattern of the mask arranged on mask switch part municipal solid waste.

[0224]As shown in drawing 21, between the electrodes 512,513 and between the electrodes 514,515 are connectable by using the mask that the metal layer 510,511 is formed with the top layer metal UM between the electrodes 512,513 and between the electrodes 514,515.

[0225]As shown in drawing 22, between the electrodes 512,513 and between the electrodes 514,515 can be intercepted by using the mask that a metal layer is not formed with the top layer metal UM between the electrodes 512,513 and between the electrodes 514,515.

[0226]In the example of drawing 21 and drawing 22, the capacity formation section C500 is thoroughly separable from an operational amplifier by providing a mask switch part in the terminal of both capacity formation sections C500, respectively.

[0227]In the circuit of the stages with an arbitrary analog-to-digital circuit in which this invention is not limited to the above-mentioned embodiment, At least one of the D/A converters which have an arithmetic amplifier which has a switchable profit, a subtraction amplifier which has a switchable profit, a sub A/D converter which has a switchable full-scale range, and a switchable full-scale range may be used.

[Translation done.]

* NOTICES *

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- 1.This document has been translated by computer. So the translation may not reflect the original precisely.
- 2.**** shows the word which can not be translated.
- 3.In the drawings, any words are not translated.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention]Here, when the voltage range of the analog input signal V_{in} is made into VIN_{p-p} , the full-scale range of sub A/D converter 9 in the 1st step of circuit 3 is equal to voltage range VIN_{p-p} of an analog input signal in the above-mentioned analog-to-digital circuit 100. The full-scale range of sub A/D converter 9 in the 2-4th step of circuit 4-6 is equal to output voltage range $VIN_{p-p}/8$ of the subtraction amplifier 14 of the 1-3rd step of circuits 3-5 respectively.

[0009]The full-scale range of D/A converter 10 in the 1st step of circuit 3 is equal to voltage range VIN_{p-p} of the analog input signal V_{in} like sub A/D converter 9. The full-scale range of the voltage of D/A converter 10 in the 2nd step and the 3rd step of circuit 4 and 5 is set to VIN_{p-p} as the full-scale range of sub A/D converter 9] $p-p$ twice many / 4 in order to take consistency with the output voltage range of the arithmetic amplifier 11 which has the profit 2.

[0010]Next, operation of the analog-to-digital circuit 1 of drawing 23 is explained. The sample hold circuit 2 samples the analog input signal V_{in} , and carries out fixed time maintenance. The analog input signal V_{in} outputted from the sample hold circuit 2 is transmitted to the 1st step of circuit 3.

[0011]In the 1st step of circuit 3, sub A/D converter 9 performs an analog to digital to the analog input signal V_{in} of voltage range VIN_{p-p} . Here, the full-scale range of sub A/D converter 9 is VIN_{p-p} as mentioned above. The digital output ($2^9, 2^8, 2^7, 2^6$) which is an analog-to-digital result of sub A/D converter 9 is transmitted to the output circuit 8 via the four latch circuitry 7 while it is transmitted to D/A converter 10. The normal output voltage range of D/A converter 10 is expressed like a following formula.

[0012]

(The 1st step of resolution-1) x(full-scale range of D/A converter 10)/(the 1st step of resolution)

$= (2^4 - 1) \times (VIN_{p-p}) / 2^4 = 15VIN_{p-p} / 16$ one side and the arithmetic amplifier 11 sample the analog input signal V_{in} , and amplify and hold it. The output voltage range of the arithmetic amplifier 11 is expressed like a following formula.

[0013]

(Voltage range VIN_{p-p} of the analog input signal V_{in}) x (profit of the arithmetic amplifier 11)

$= \text{The } VIN_{p-p} \times 1 = VIN_{p-p}$ subtraction amplifier 14 subtracts and amplifies the analog input signal V_{in} and the D/A conversion result of D/A converter 10 which were outputted from the arithmetic amplifier 11. The output of the subtraction amplification width circuit 14 is transmitted to the 2nd step of circuit 4. The output voltage range of the 1st step of subtraction amplifier 14 is expressed like a following formula.

[0014]

(Output voltage range of the arithmetic amplifier 11) x (- (normal output voltage range of D/A converter 10)) (profit of the subtraction amplifier 14)

$= (VIN_{p-p}) (- (15VIN_{p-p}/16))$ In the $x2 = VIN_{p-p}/82$ step circuit 4, sub A/D converter 9 performs an A/D conversion to the output of the subtraction amplifier 14 of the 1st step of circuit 3. The A/D conversion result of sub A/D converter 9 is transmitted to the output circuit 8 via the three latch circuitry 7 while it is transmitted to D/A converter 10. Thereby, a 2-bit digital output ($2^5, 2^4$) is obtained at least for Nakagami from the 2nd step of circuit 4. The normal output voltage range of D/A converter 10 is expressed like a following formula.

[0015]

(The 2nd step of resolution-1) \times (full-scale range of D/A converter 10) / (the 2nd step of resolution)

$= (2^2 - 1) \times (VIN_{p-p}/4) / 2^2 = 3VIN_{p-p}/16$ one side and the arithmetic amplifier 11 amplify the output of the arithmetic amplifier 13 of the 1st step of circuit 3. The output voltage range of the arithmetic amplifier 11 is expressed like a following formula.

[0016]

(Output voltage range of the 1st step of subtraction amplifier 14) \times (profit of the arithmetic amplifier 11)

$= (VIN_{p-p}/8)$ The $x2 = VIN_{p-p}/4$ subtraction amplifier 14 subtracts and amplifies the output of the arithmetic amplifier 11, and the D/A conversion result of D/A converter 10. The output of the subtraction amplifier 14 is transmitted to the 3rd step of circuit 5. The range of the output voltage of the 2nd step of subtraction amplifier 14 is expressed like a following formula.

[0017]

(Output voltage range of the arithmetic amplifier 11) \times (- (normal output voltage range of D/A converter 10)) (profit of the subtraction amplifier 14)

$= (VIN_{p-p}/4) (- (3VIN_{p-p}/16))$ In the $x2 = VIN_{p-p}/83$ step circuit 5, the same operation as the 2nd step of circuit 4 is performed to the output of the subtraction amplifier 14 of the 2nd step of circuit 3. Thereby, a 2-bit digital output ($2^3, 2^2$) is obtained at least for Nakashita from the 3rd step of circuit 5. The output voltage range of each part is the same as that of the 2nd step of circuit 4.

[0018] In the 4th step of circuit 6, sub A/D converter 9 performs an A/D conversion to the output of the subtraction amplifier 14 of the 3rd step of circuit 5, and the digital output ($2^1, 2^0$) of 2 bits of low ranks is obtained.

[0019] The digital output of the 1st step - the 4th step of circuits 3-6 arrives at the output circuit 8 simultaneously through each latch circuitry 7. That is, each latch circuitry 7 is formed in order to take the synchronization of the digital output of each circuits 3-6.

[0020] The output circuit 8 carries out the after [a digital compensation process] parallel output of the 10-bit digital output Dout of the analog input signal Vin, when required.

[0021] Thus, even if the conversion number of bits increases and LSB (Least Significant Bit) becomes small with reduction in power supply voltage, the resolution of sub A/D converter 9 can be raised and sufficient conversion precision is acquired.

[0022] Drawing 24 (a) is a figure for the circuit diagram and drawing 24 (b) in which the composition of the subtraction amplifier of the analog-to-digital circuit of drawing 23 is shown to explain operation of the subtraction amplifier of drawing 24 (a).

[0023] In drawing 24, the inversed input terminal of the operational amplifier 101 is connected to the node nb, and the non-inversed input terminal is grounded. The output terminal of the operational amplifier 101 is connected to the inversed input terminal via the capacitor 102 while being connected to the node no. Switch SW1 is connected between the inversed input terminal of the operational amplifier 1, and a non-inversed input terminal, and the capacitor 103 is connected between the node nb and the node na. It is connected to the node n1 via switch SW2, and the node na is connected to the node n2 via switch SW3. These switch SW2 and SW3 are constituted by the CMOS switch which usually consists of a CMOS (complementary-type metal oxide semiconductor) field effect transistor.

[0024] Voltage V_1 is inputted into the node n1, voltage V_2 is inputted into the node n2, and

voltage V_O is outputted from the node no.

[0025] Here, operation of the subtraction amplifier of drawing 24 (a) is explained, referring to drawing 24 (b). Capacity value of the capacitor 101 is set to C , capacity value of the capacitor 103 is set to KC , and earth potentials are made into V_G . K is a constant.

[0026] First, switch SW1 and switch SW2 are made one, and switch SW3 is turned OFF. Thereby, the voltage of the node na serves as V_1 . The voltage of the node no is set to 0. At this time, the electric charge Q_a of the node nb becomes like a following formula.

[0027] After turning OFF $Q_a = (V_G - V_1) KC$, next switch SW1, switch SW2 is turned OFF and switch SW3 is made one. Thereby, the voltage of the node na serves as V_2 . The voltage of the node no serves as V_O . In order to carry out the imaginary earth of the node nb at this time, the electric charge Q_b of the node nb becomes like a following formula.

[0028] Since there is no course out of which an electric charge escapes from and comes in the $Q_b = (V_G - V_2) KC + (V_G - V_O) C$ node nb, it becomes $Q_a = Q_b$ with conservation of charge. Therefore, a following formula is materialized.

[0029] $(V_G - V_1) KC = (V_G - V_2) KC + (V_G - V_O) C$ top type to the node no becomes like a following formula.

[0030] Voltage V_2 is subtracted from $V_O = V_G + (V_1 - V_2) K$, thus voltage V_1 , and the subtraction value is amplified K times.

[0031] Therefore, a subtraction amplifier has a function which outputs the difference of voltage V_1 and voltage V_2 by the profit decided by the capacity factor of the capacitor 103 and the capacitor 102. For example, a sample hold function 1 time the profit of this will be given to a subtraction amplifier by setting it as $KC = C$ ($K = 1$).

[0032] Drawing 25 is a figure showing the composition of the sub A/D converter used in the analog-to-digital circuit of drawing 23.

[0033] Two or more comparators 900 are arranged in the parallel connected type analog-digital converter 9 of drawing 25. The analog input voltage V_{in} is given to one input terminal of two or more comparators 900, and the reference voltage obtained by carrying out the partial pressure of the voltage between the high potential side reference voltage V_{RT} and the low voltage side reference voltage V_{RB} to the input terminal of another side by two or more resistance R is given, respectively. Each comparator 900 compares the voltage of one input terminal with the voltage of the input terminal of another side. The digital code D_{code} can be obtained by encoding the comparison result of two or more comparators 900 with the encoder 910.

[0034] By the way, when the voltage range of the analog input signal given to an analog-to-digital circuit is changed, Or to change the method of the analog input signal given to an analog-to-digital circuit in a differential double end input and a single-ended input, it is necessary to change the specification of an analog-to-digital circuit.

[0035] Here, a differential double end input and a single-ended input are explained. Drawing 26 (a) and (b) is a figure for explaining the analog to digital in a differential double end input and a single-ended input. A horizontal axis shows the analog input voltage V_{IN} , and a vertical axis shows the outputted digital code D_{code} .

[0036] As shown in drawing 26 (a), at the time of a differential double end input, the right side analog input voltage $V_{in}(+)$ and the negative side analog input voltage $V_{in}(-)$ of the analog input signal V_{in} change complementarily. Thereby, the difference of the right side analog input voltage $V_{in}(+)$ and the negative side analog input voltage $V_{in}(-)$ serves as voltage range $V_{IN_{p-p}}$ of the analog input signal V_{in} .

[0037] Therefore, as shown in drawing 26 (a), the right side analog input voltage $V_{in}(+)$ changes from 1.0V in 2.0, When the negative side analog input voltage $V_{in}(-)$ changes in 2.0V to 1.0V, the voltage range of the analog input signal V_{in} is set to 2.0V from the operation of $V_{in}(+) - V_{in}(-)$.

[0038] On the other hand, as shown in drawing 26 (b), at the time of a single-ended input, the

right side analog input voltage V_{in} (+) changes. Thereby, the voltage range of the right side analog input voltage V_{in} (+) turns into a voltage range of the analog input signal V_{in} .

[0039]Therefore, as shown in drawing 26 (b), when the right side analog input voltage V_{in} (+) changes in 1.0V to 2.0V, the voltage range of an analog input signal is set to 1.0V.

[0040]That is, if the voltage range of the analog input signal V_{in} of a differential double end input method is made into $2V_{IN_{p-p}}$, the voltage range of the analog input signal V_{in} of a single-ended input method will serve as $V_{IN_{p-p}}$.

[0041]Thus, with a differential double end input method and a single-ended input method, even if the range of change of each analog input voltage is the same, the voltage ranges of an analog input signal will differ.

[0042]In the above-mentioned conventional analog-to-digital circuit, when changing the voltage range of an analog input signal, or when changing the input method of an analog input signal, it is necessary to redesign circuitry.

[0043]The purpose of this invention is to provide the pipeline type analog-to-digital circuit which can change the input method between change of the voltage range of an analog input signal or a differential double end input, and a single-ended input easily without redesigning circuitry.

[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1]It is a block diagram showing the composition of the pipeline type analog-to-digital circuit in a 1st embodiment of this invention.

[Drawing 2]It is a figure showing setting out in the case of changing the analog-to-digital circuit of drawing 1 to a differential double end input method and a single-ended input method, respectively.

[Drawing 3]It is a block diagram showing the composition of the pipeline type analog-to-digital circuit in a 2nd embodiment of this invention.

[Drawing 4]It is a circuit diagram showing the 1st example of the composition of the arithmetic amplifier in the analog-to-digital circuit of drawing 1.

[Drawing 5]It is a circuit diagram showing the 2nd example of the composition of the arithmetic amplifier in the analog-to-digital circuit of drawing 1.

[Drawing 6]It is a circuit diagram showing the 1st example of the concrete circuitry of an arithmetic amplifier.

[Drawing 7]It is a circuit diagram showing the 2nd example of the concrete circuitry of an arithmetic amplifier.

[Drawing 8]It is a circuit diagram showing the 3rd example of the concrete circuitry of an arithmetic amplifier.

[Drawing 9]It is a circuit diagram showing the 4th example of the concrete circuitry of an arithmetic amplifier.

[Drawing 10]It is a circuit diagram showing the 5th example of the concrete circuitry of an arithmetic amplifier.

[Drawing 11]It is a circuit diagram showing the 6th example of the concrete circuitry of an arithmetic amplifier.

[Drawing 12]It is a circuit diagram showing the 1st example of the composition of the sub A/D converter in the analog-to-digital circuit of drawing 1.

[Drawing 13]It is a circuit diagram showing the composition of the comparator used for the sub A/D converter of drawing 12.

[Drawing 14]It is a circuit diagram showing the 2nd example of the composition of the sub A/D converter in the analog-to-digital circuit of drawing 1.

[Drawing 15]It is a circuit diagram showing the composition of the comparator used for the sub A/D converter of drawing 14.

[Drawing 16]It is a circuit diagram of the sub A/D converter in the 2nd step of circuit in the analog-to-digital circuit of drawing 3.

[Drawing 17]It is a circuit diagram of the D/A converter in the 2nd step of circuit in the analog-to-digital circuit of drawing 3.

[Drawing 18]It is a circuit diagram showing the 1st example of the composition of the subtraction amplifier in the analog-to-digital circuit of drawing 3.

[Drawing 19]It is a circuit diagram showing the 2nd example of the composition of the subtraction amplifier in the analog-to-digital circuit of drawing 3.

[Drawing 20]It is a circuit diagram showing other examples of the switch part of a switching

means.

[Drawing 21] It is the top view and sectional view showing the example of further others of the switch part of a switching means.

[Drawing 22] It is the top view and sectional view showing the example of further others of the switch part of a switching means.

[Drawing 23] It is a block diagram showing the conventional analog-to-digital circuit.

[Drawing 24] It is a figure for explaining operation of the circuit diagram showing the composition of the subtraction amplifier of the analog-to-digital circuit of drawing 23, and its subtraction amplifier.

[Drawing 25] It is a figure showing the composition of the sub A/D converter used in the analog-to-digital circuit of drawing 23.

[Drawing 26] It is a figure for explaining the analog to digital in a differential double end input and a single-ended input.

[Description of Notations]

1 Analog-to-digital circuit

3-6 The 1st step - the 4th step of circuit

9, 9a, and 9b Sub A/D converter

10 and 10b D/A converter

11, 13, and 13a Arithmetic amplifier

12 Subtractor circuit

14 14a Subtraction amplifier

VRT, VRT2, and VRT3 The high potential side reference voltage

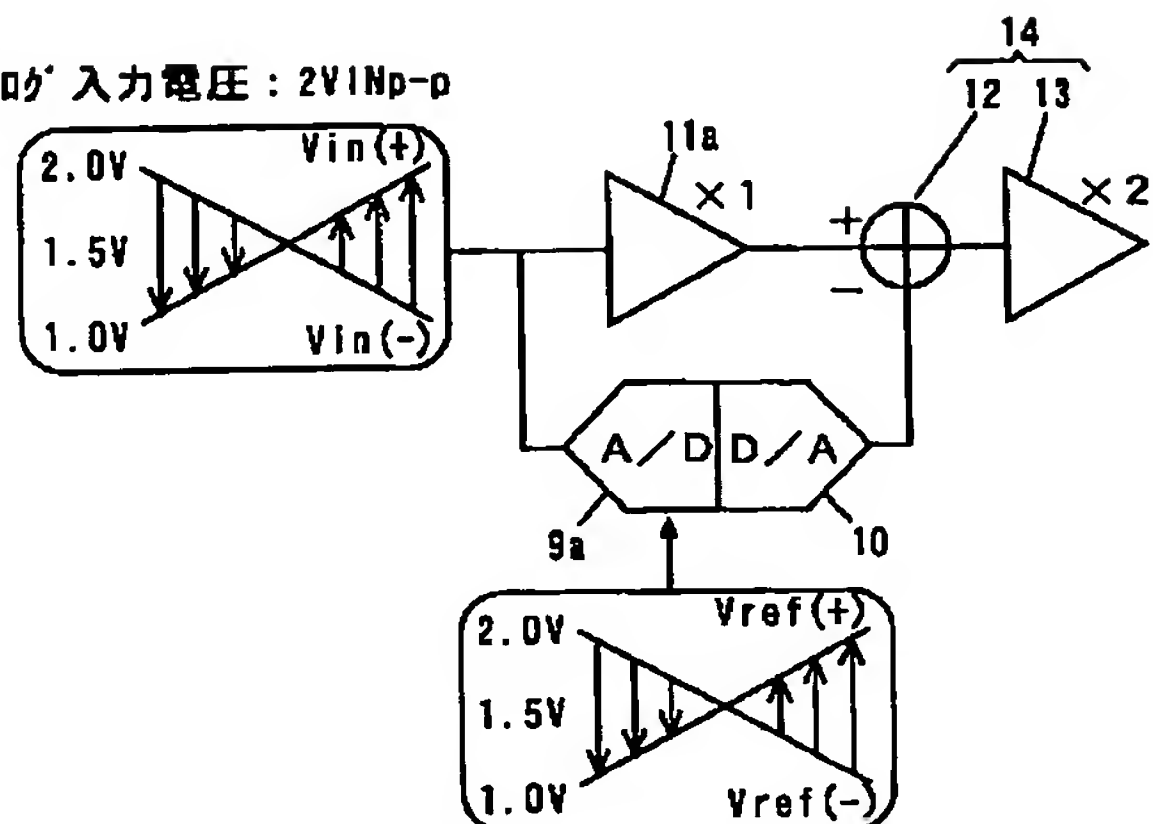
VRB, VRB2, and VRB3 The low voltage side reference voltage

VRT1 Middle reference voltage

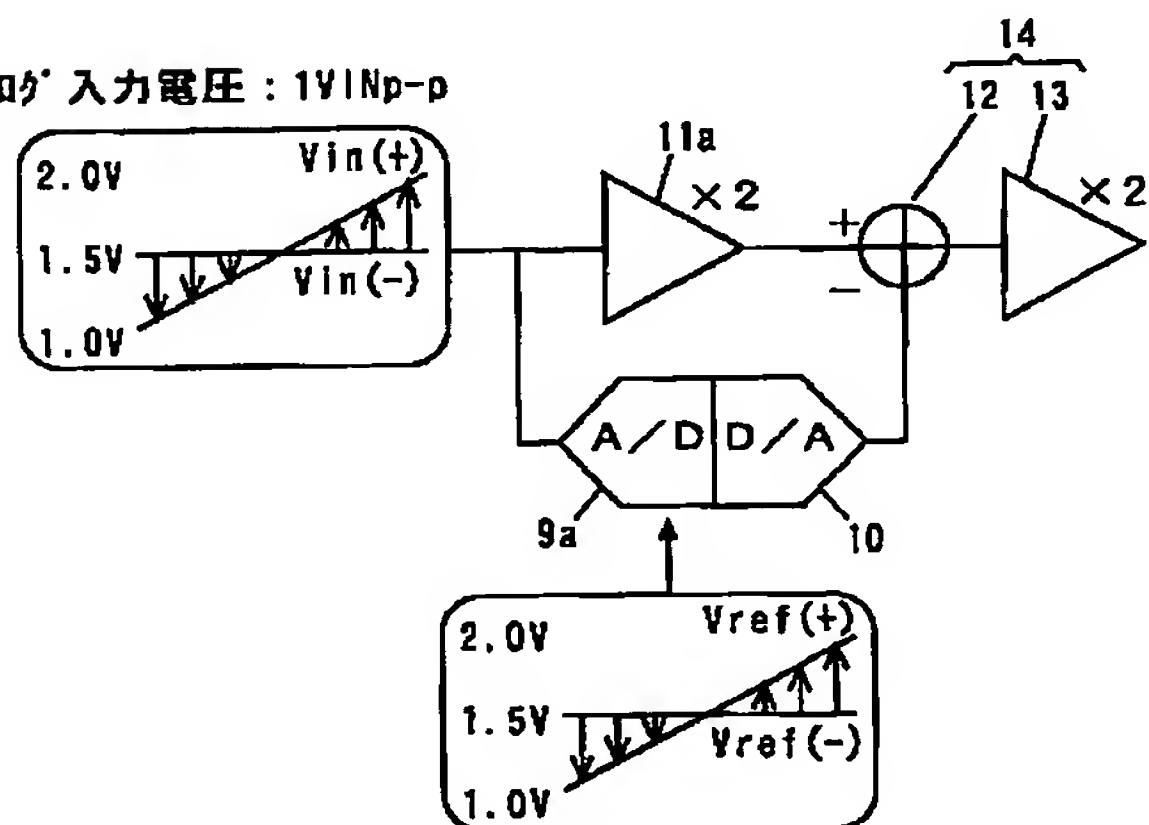
Sa, S1a, S1b, S24, S25, S26, S26, S28, S29, S30, and S31 Switch

[Translation done.]

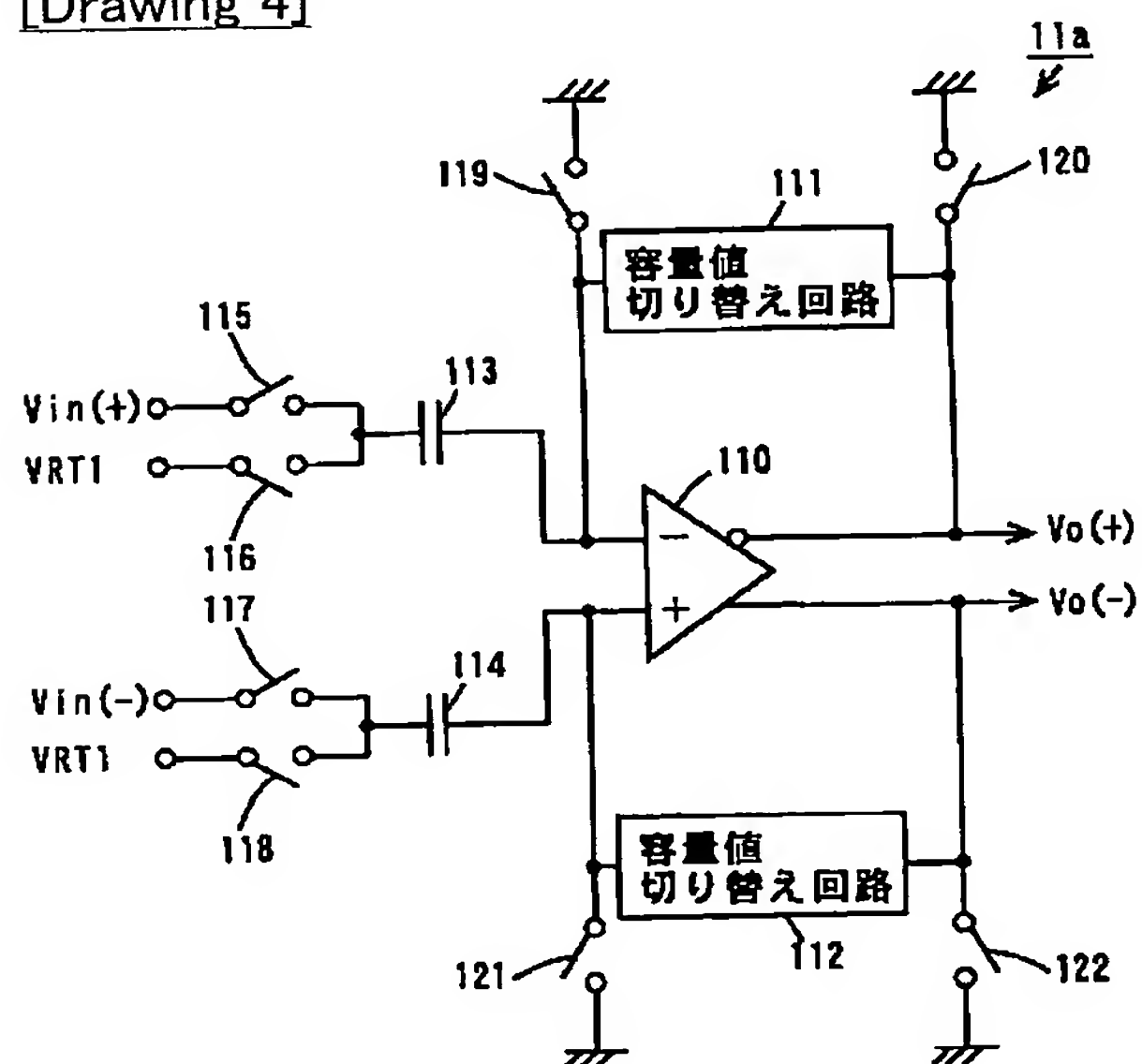
(a)

対称入力電圧: $2V_{INp-p}$ 

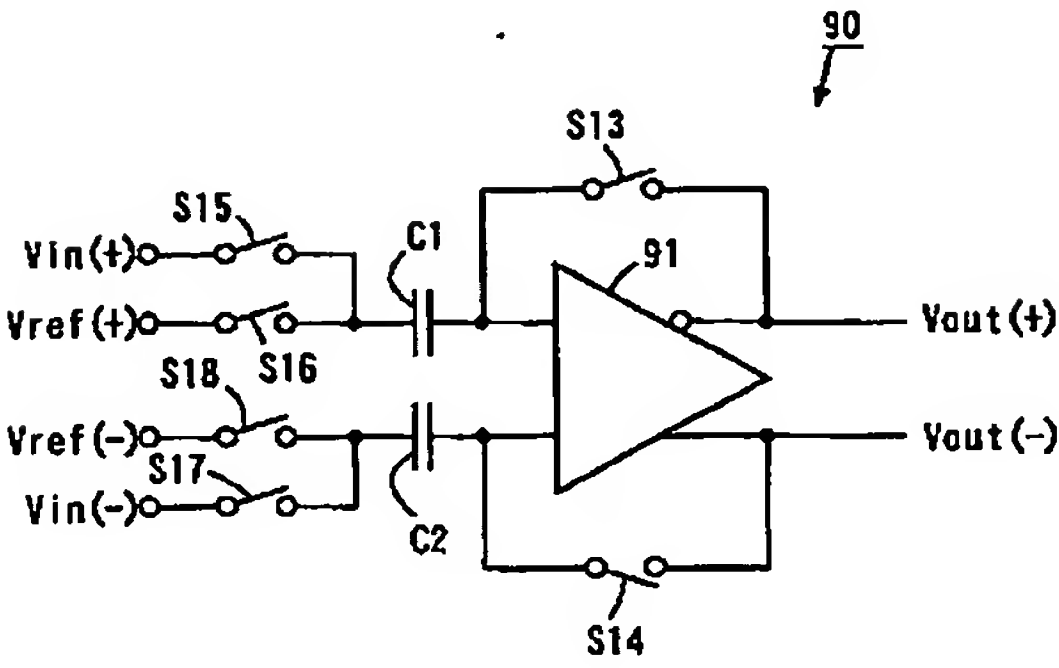
(b)

対称入力電圧: $1V_{INp-p}$ 

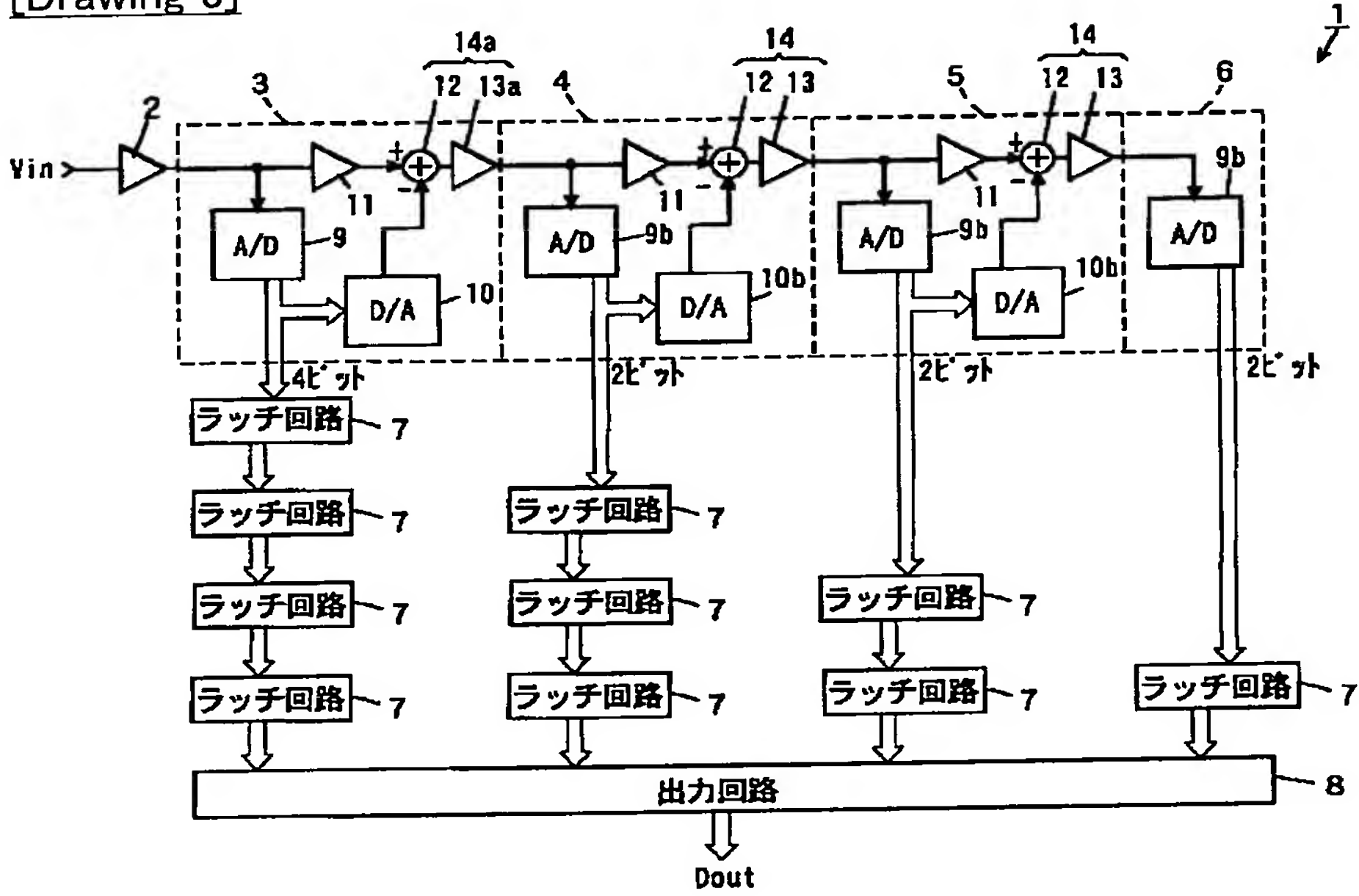
[Drawing 4]



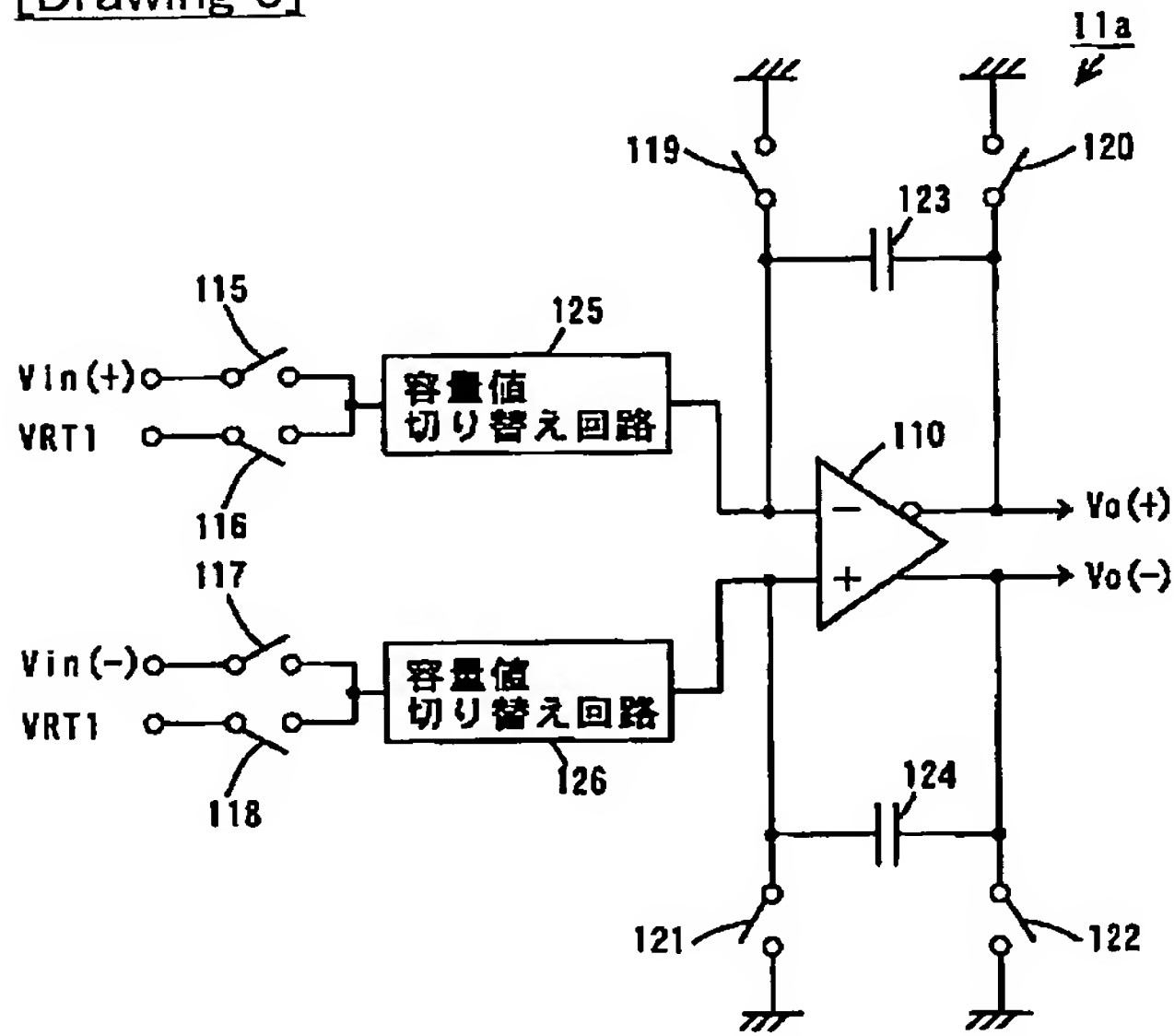
[Drawing 13]



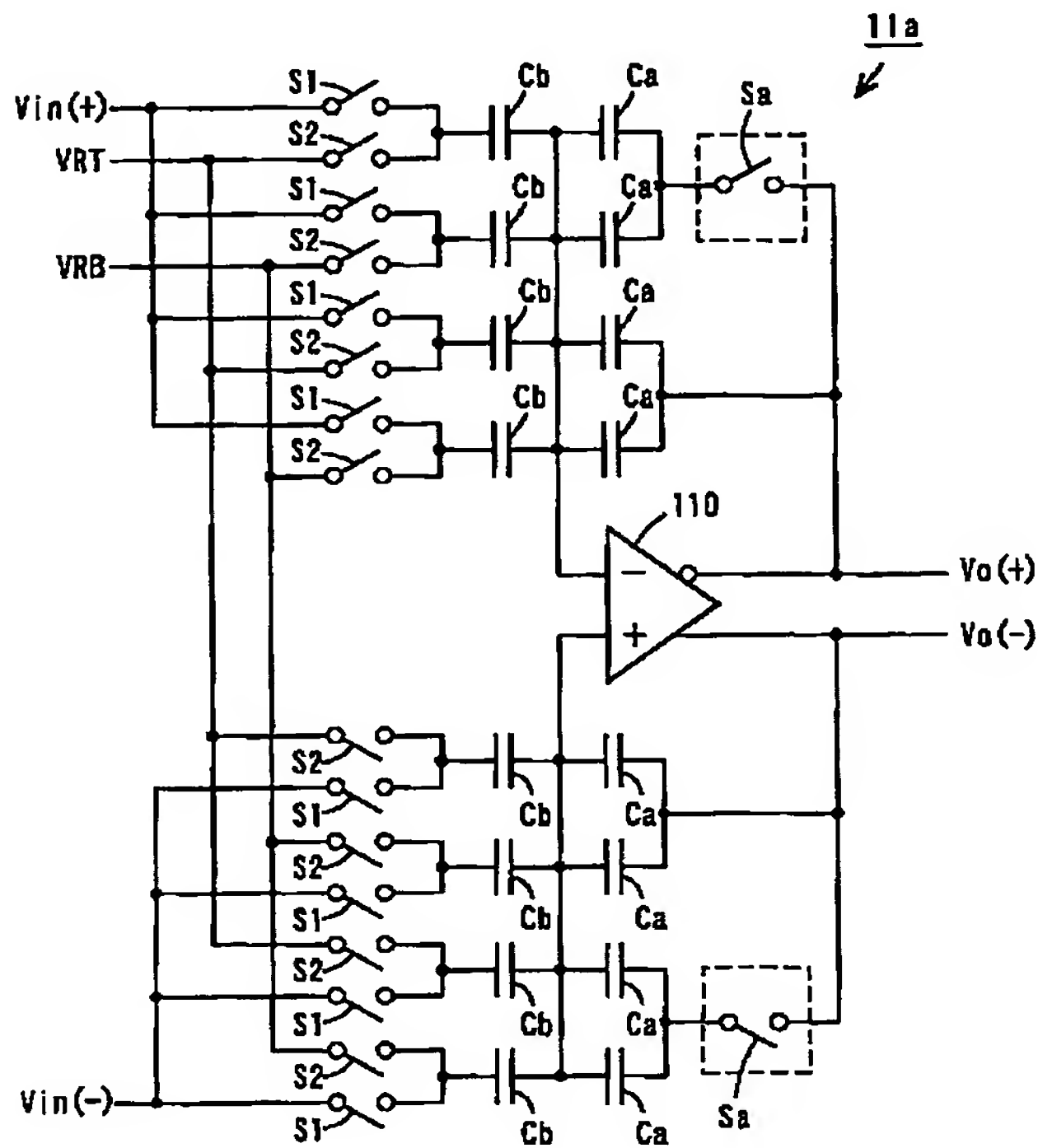
[Drawing 3]



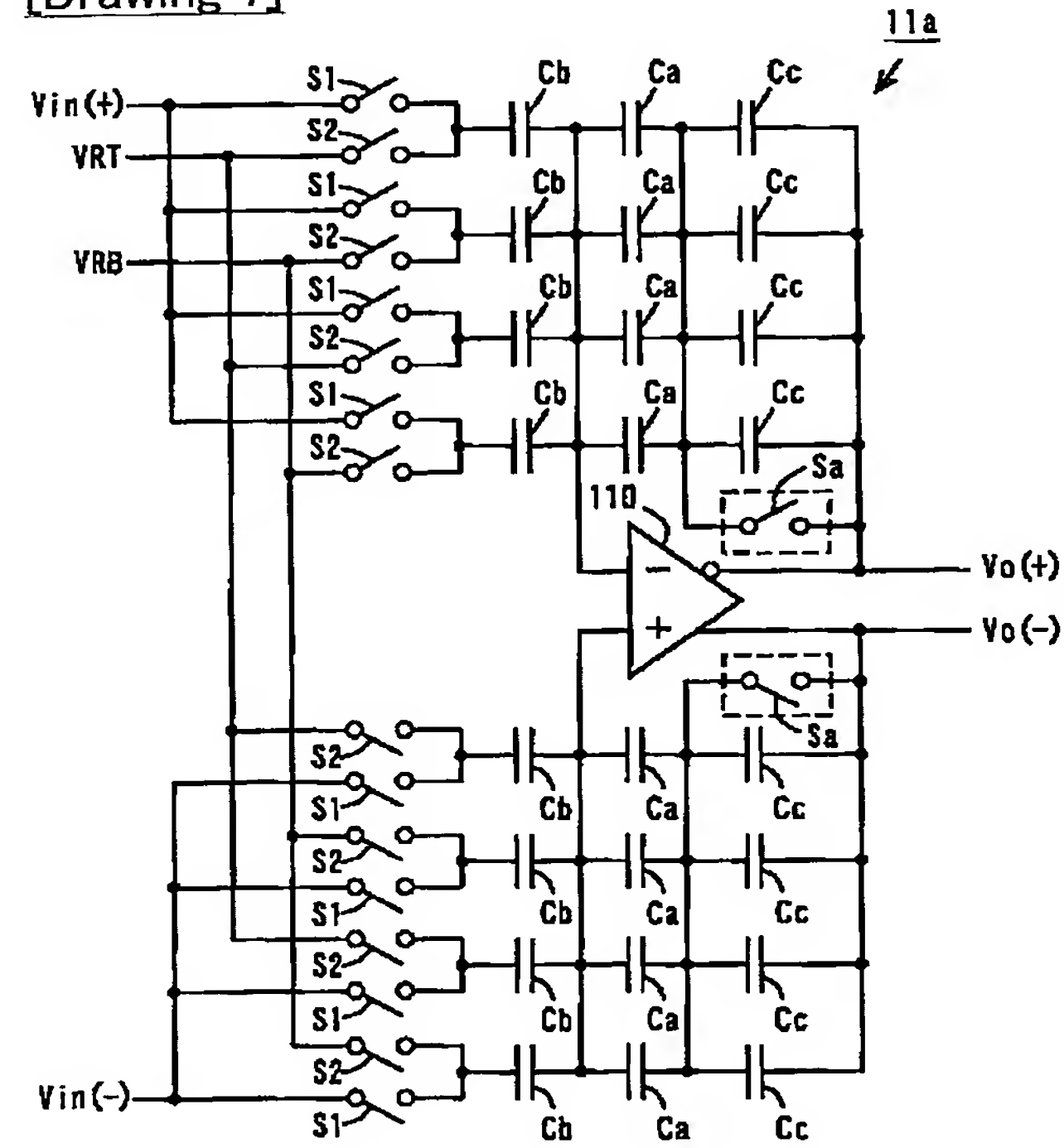
[Drawing 5]



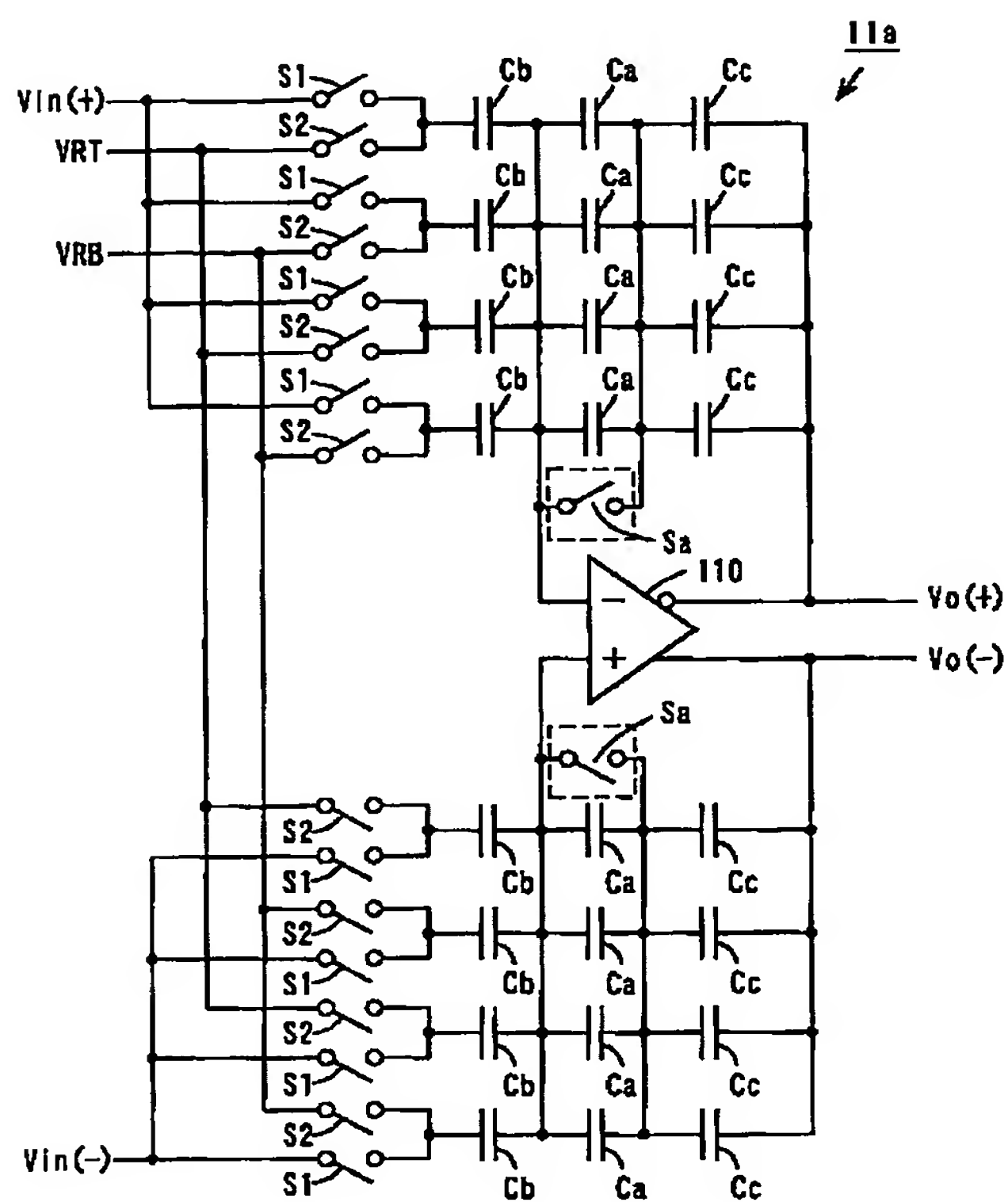
[Drawing 6]



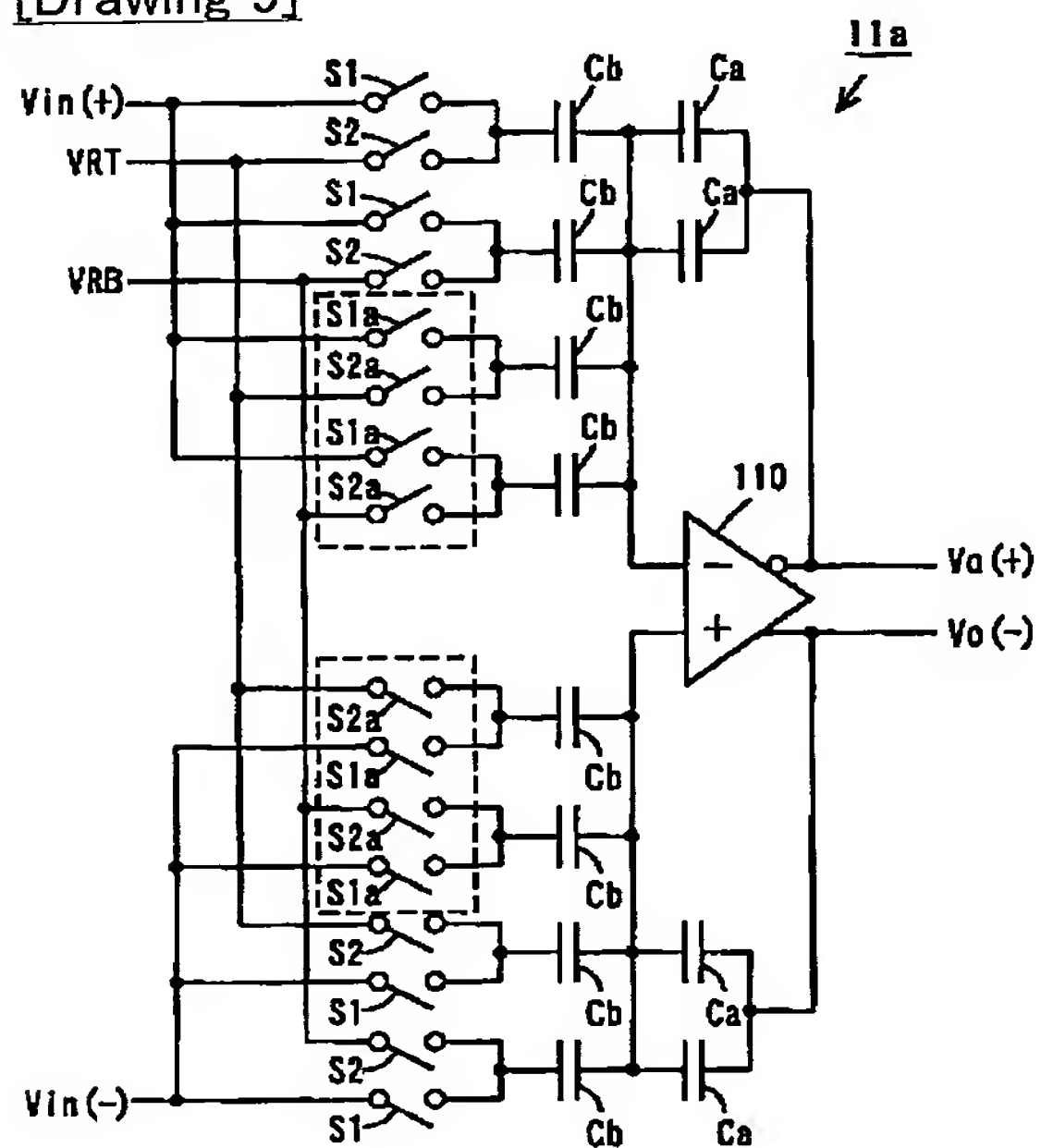
[Drawing 7]



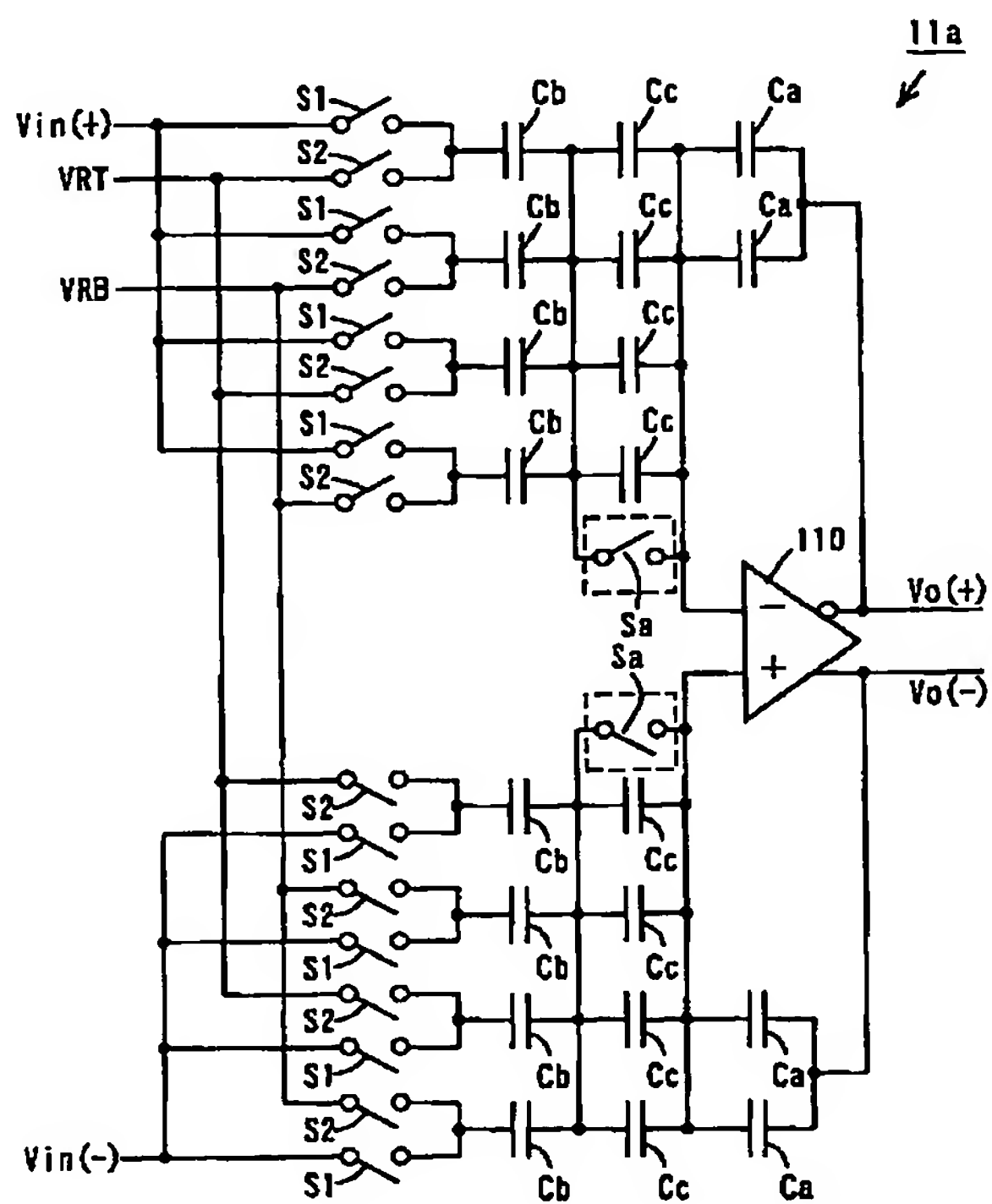
[Drawing 8]



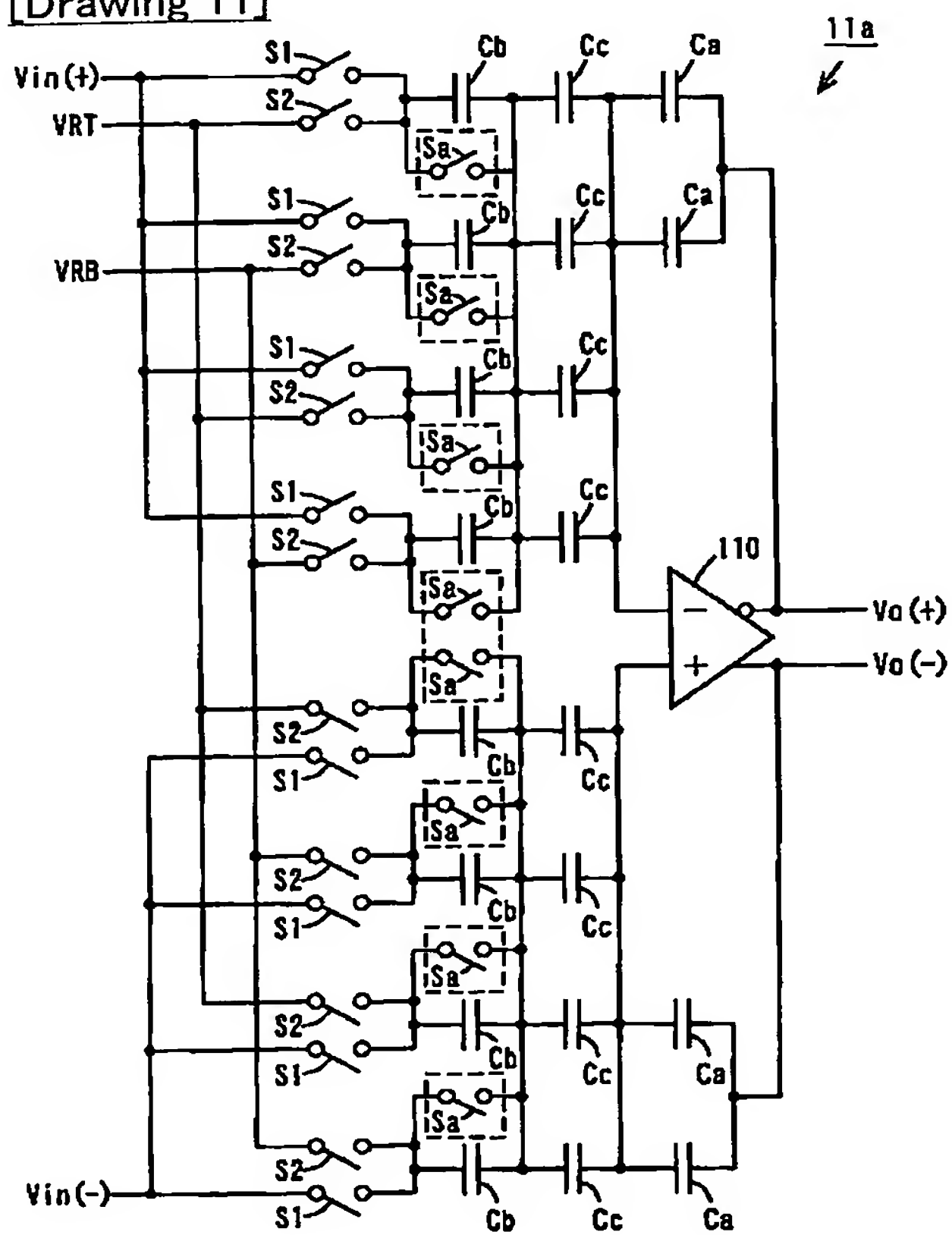
[Drawing 9]



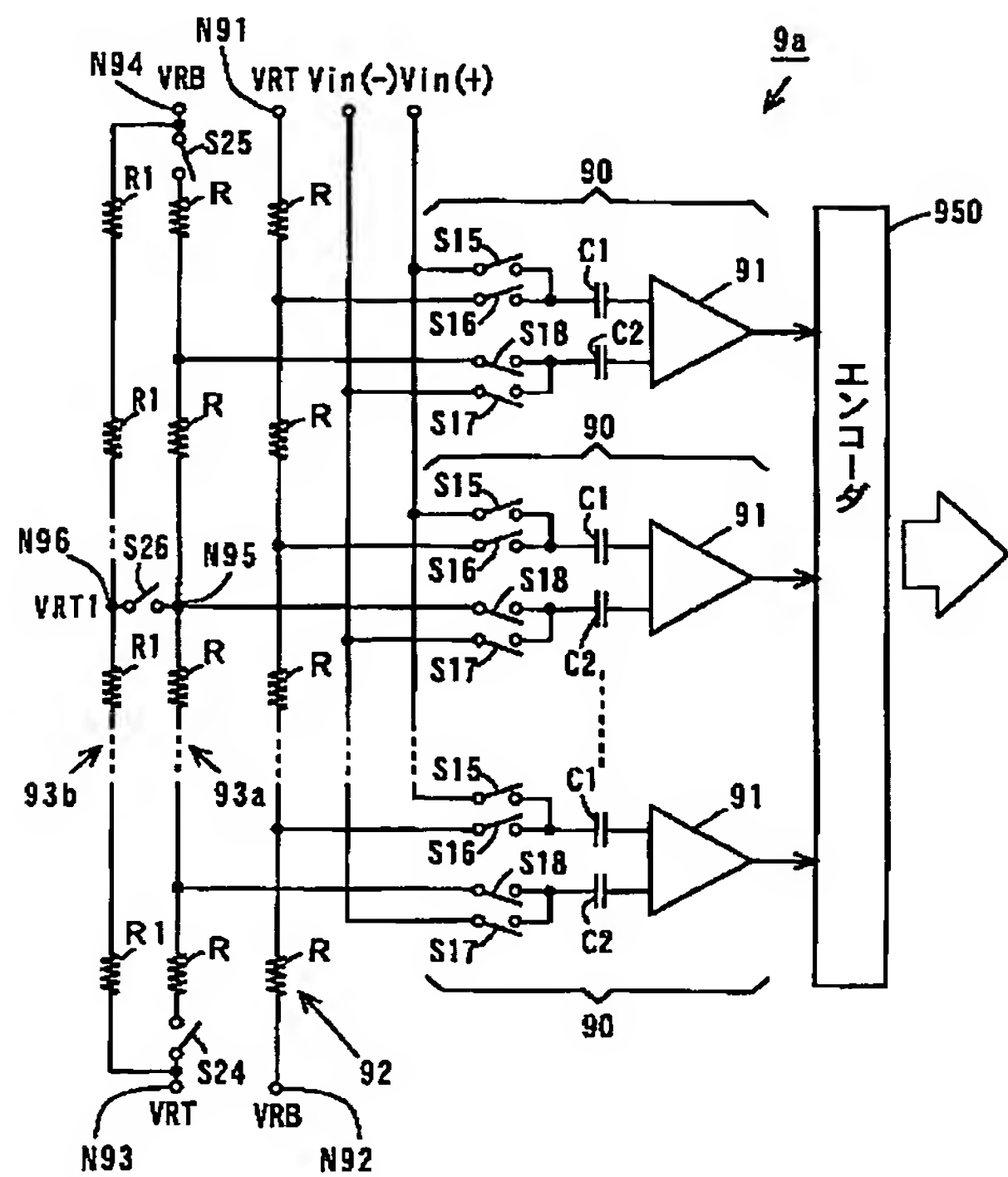
[Drawing 10]



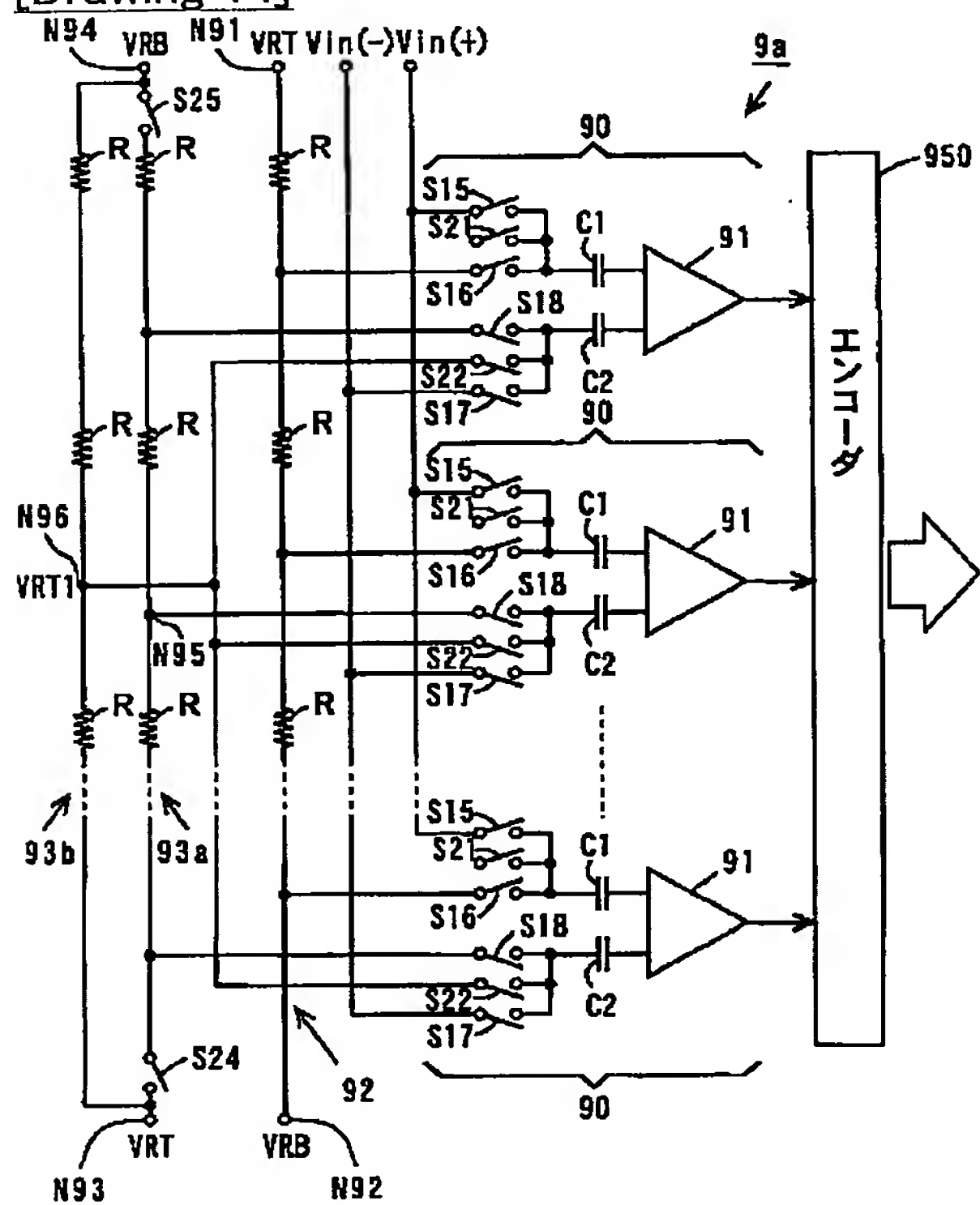
[Drawing 11]



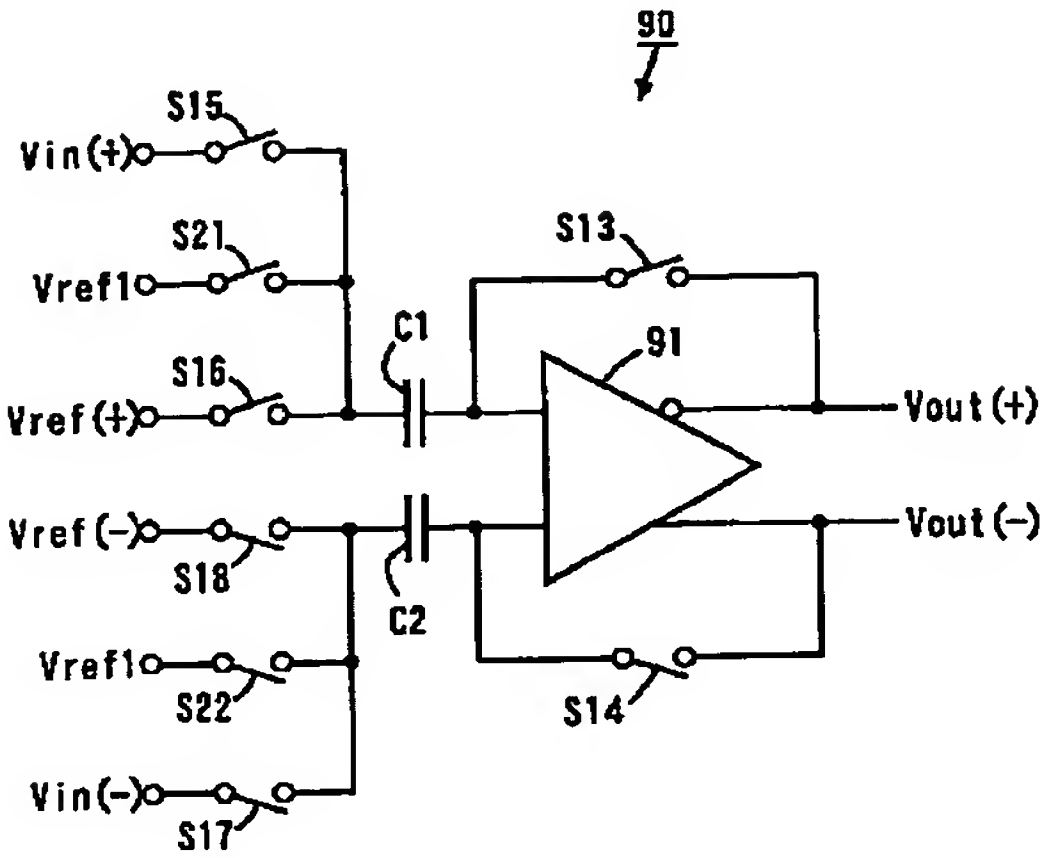
[Drawing 12]



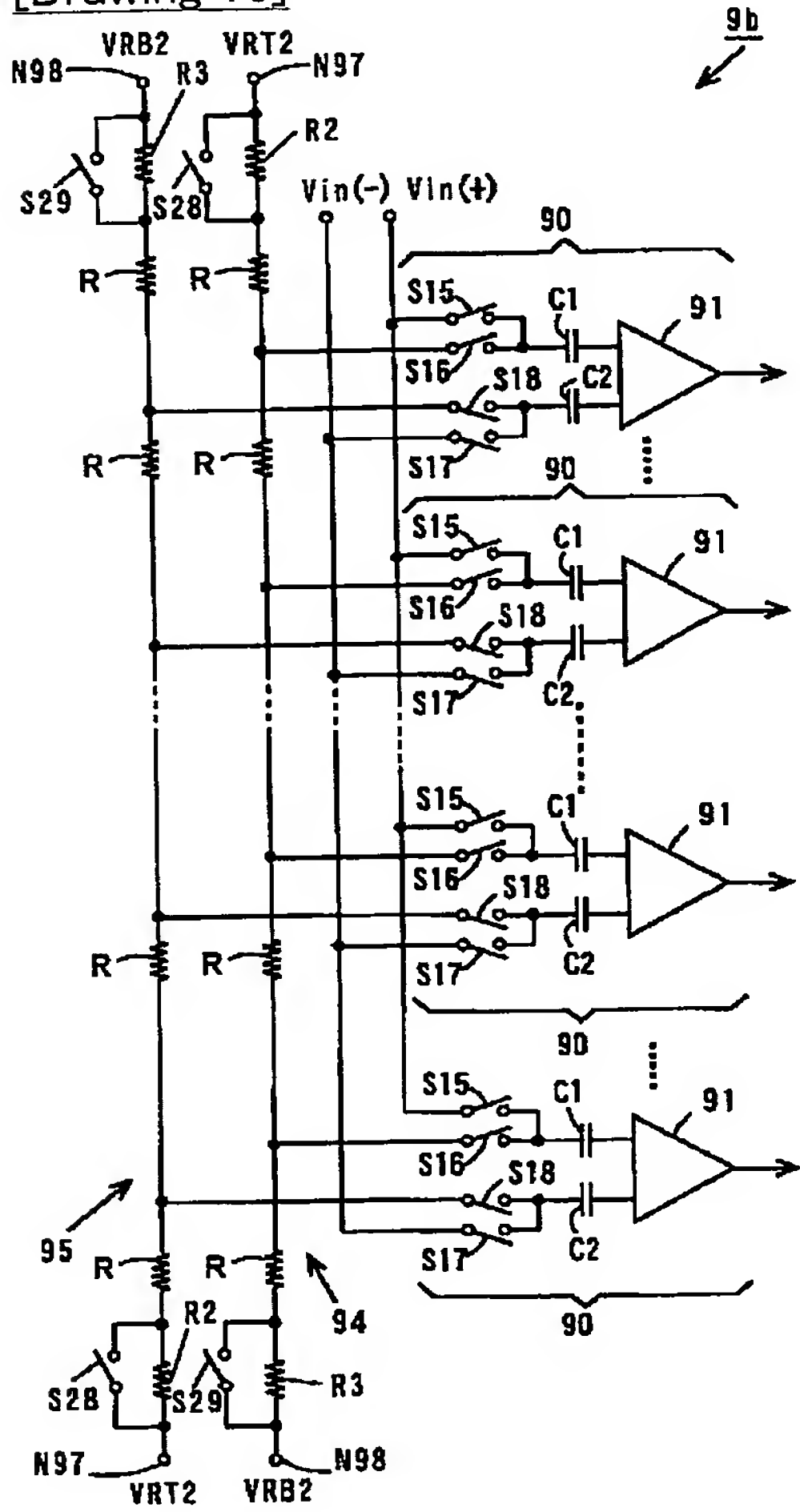
[Drawing 14]



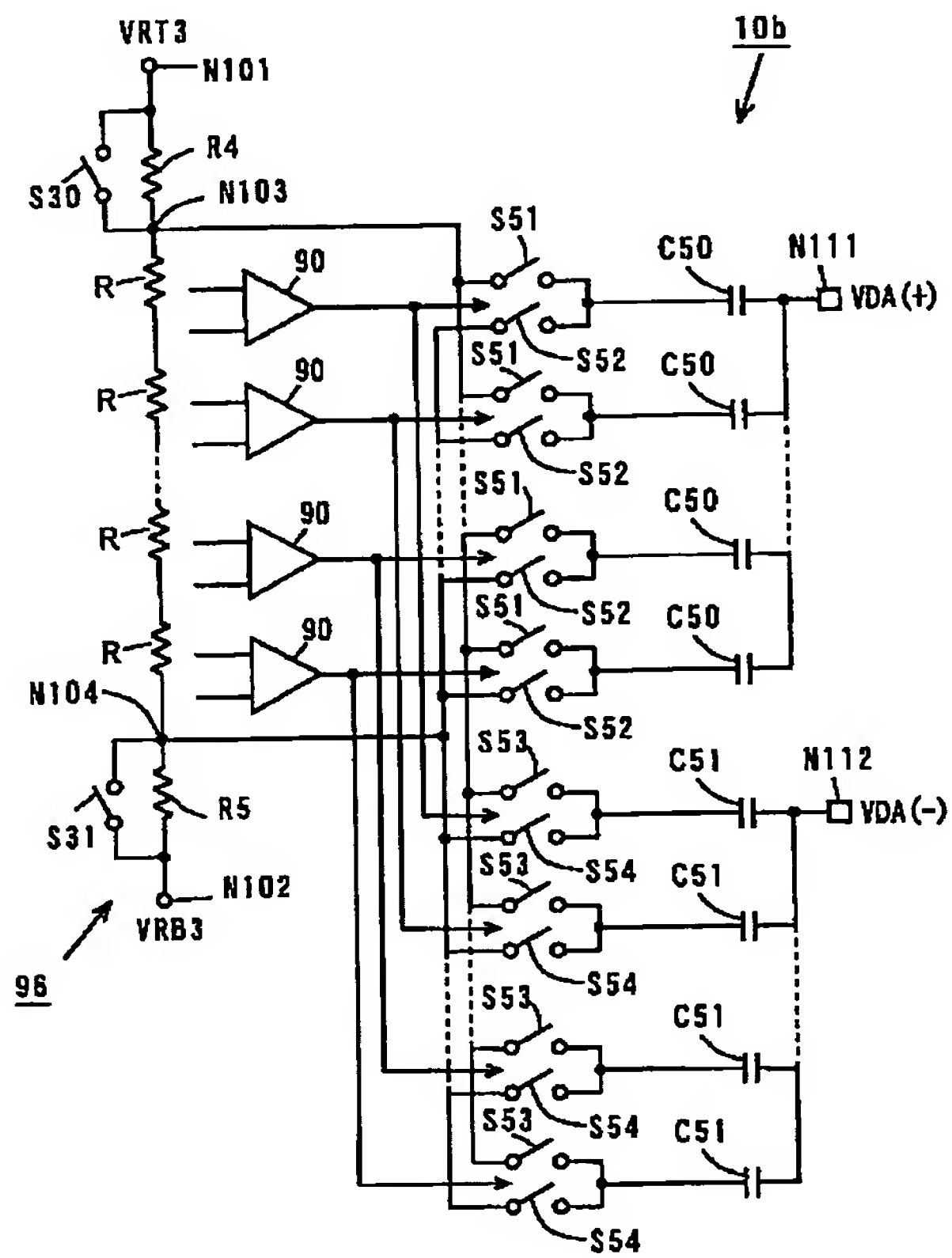
[Drawing 15]



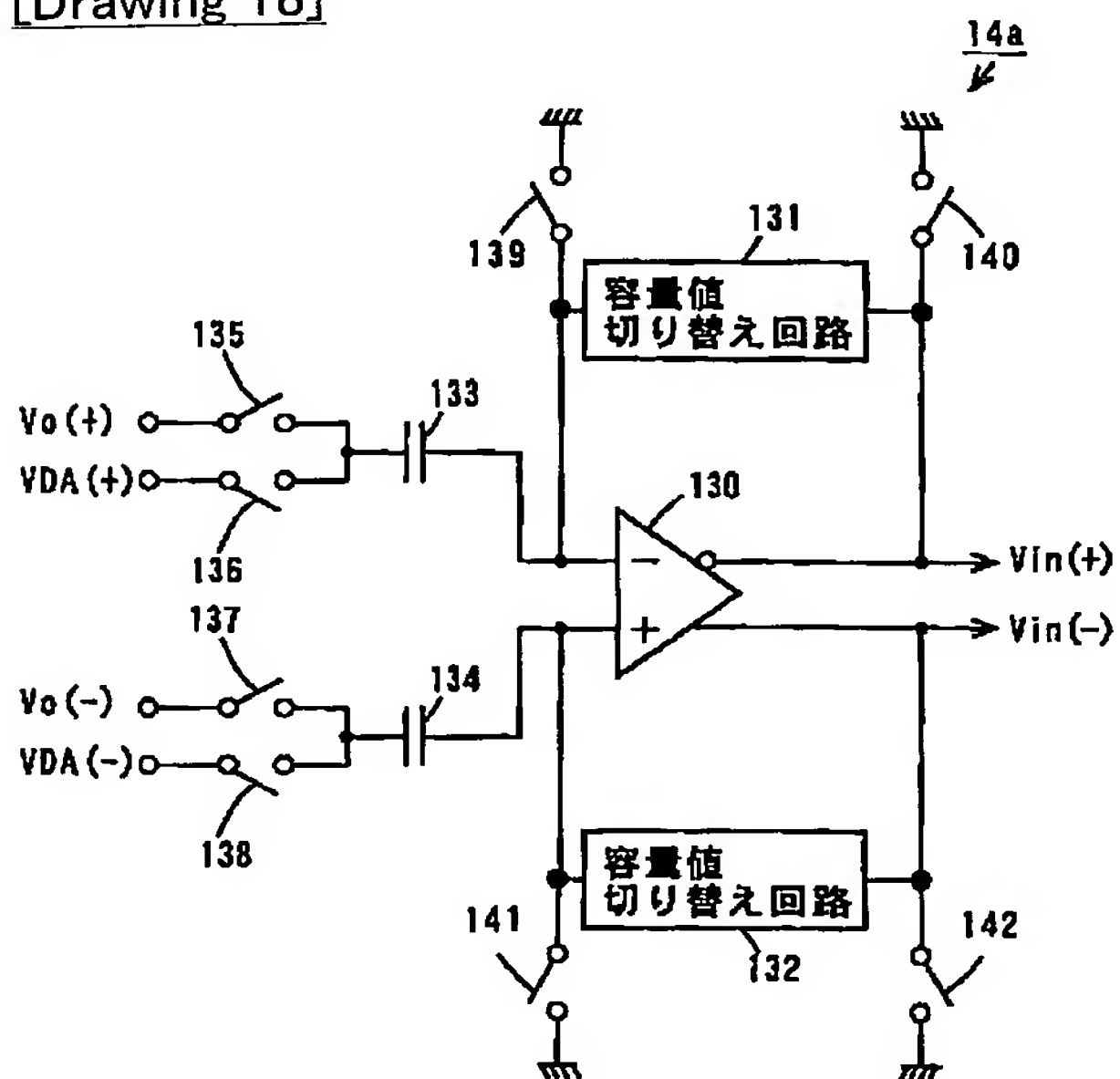
[Drawing 16]



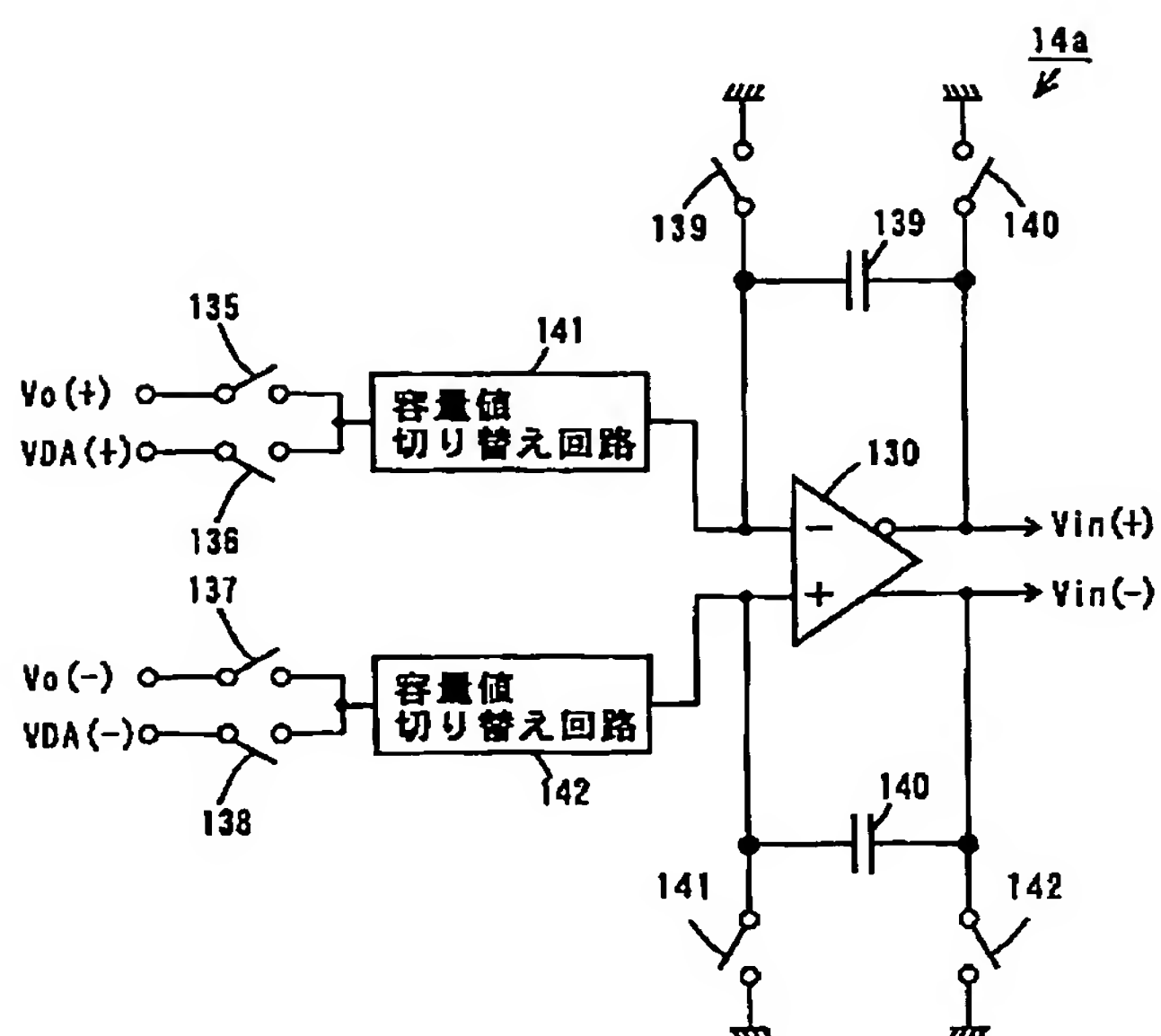
[Drawing 17]



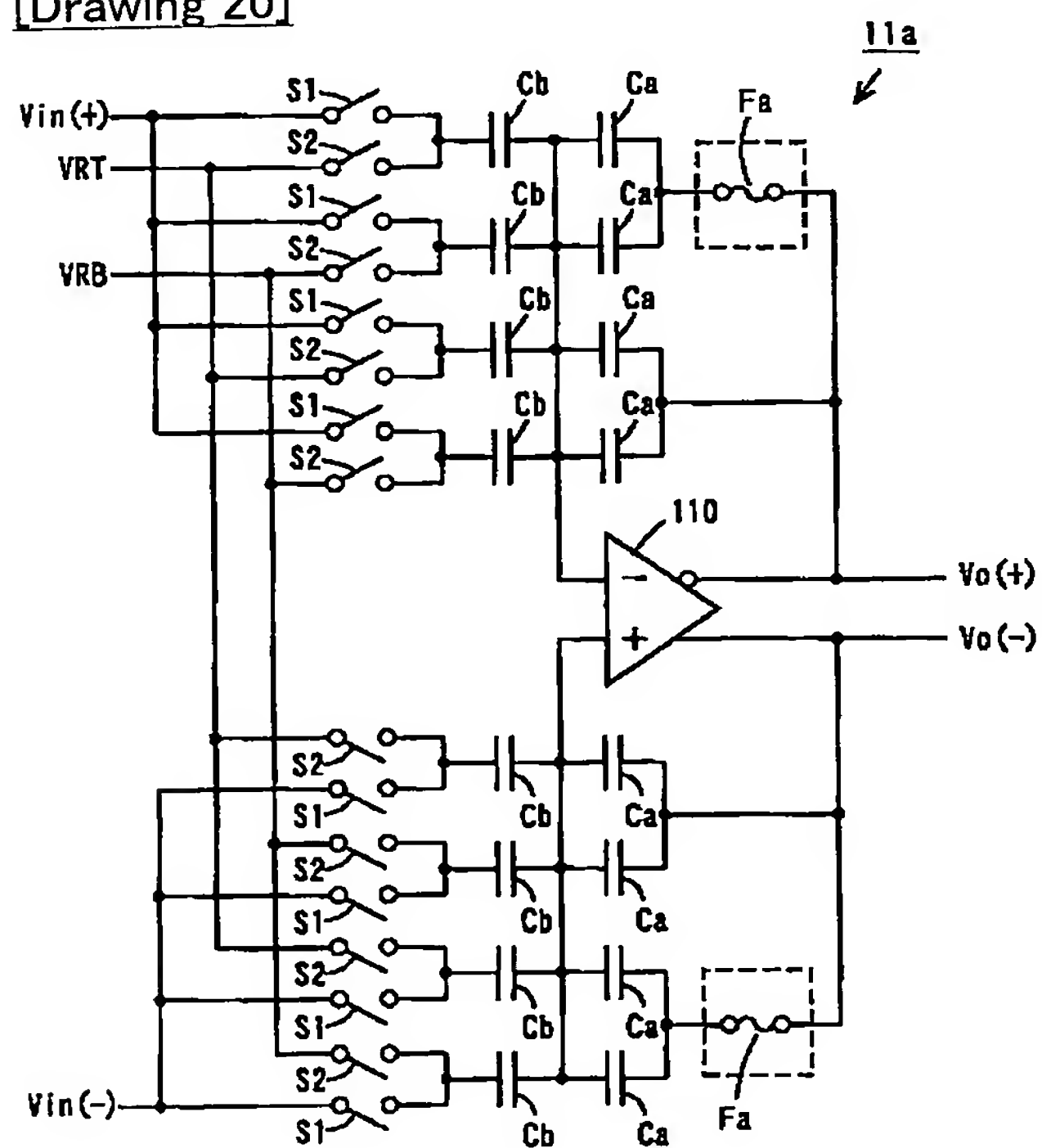
[Drawing 18]



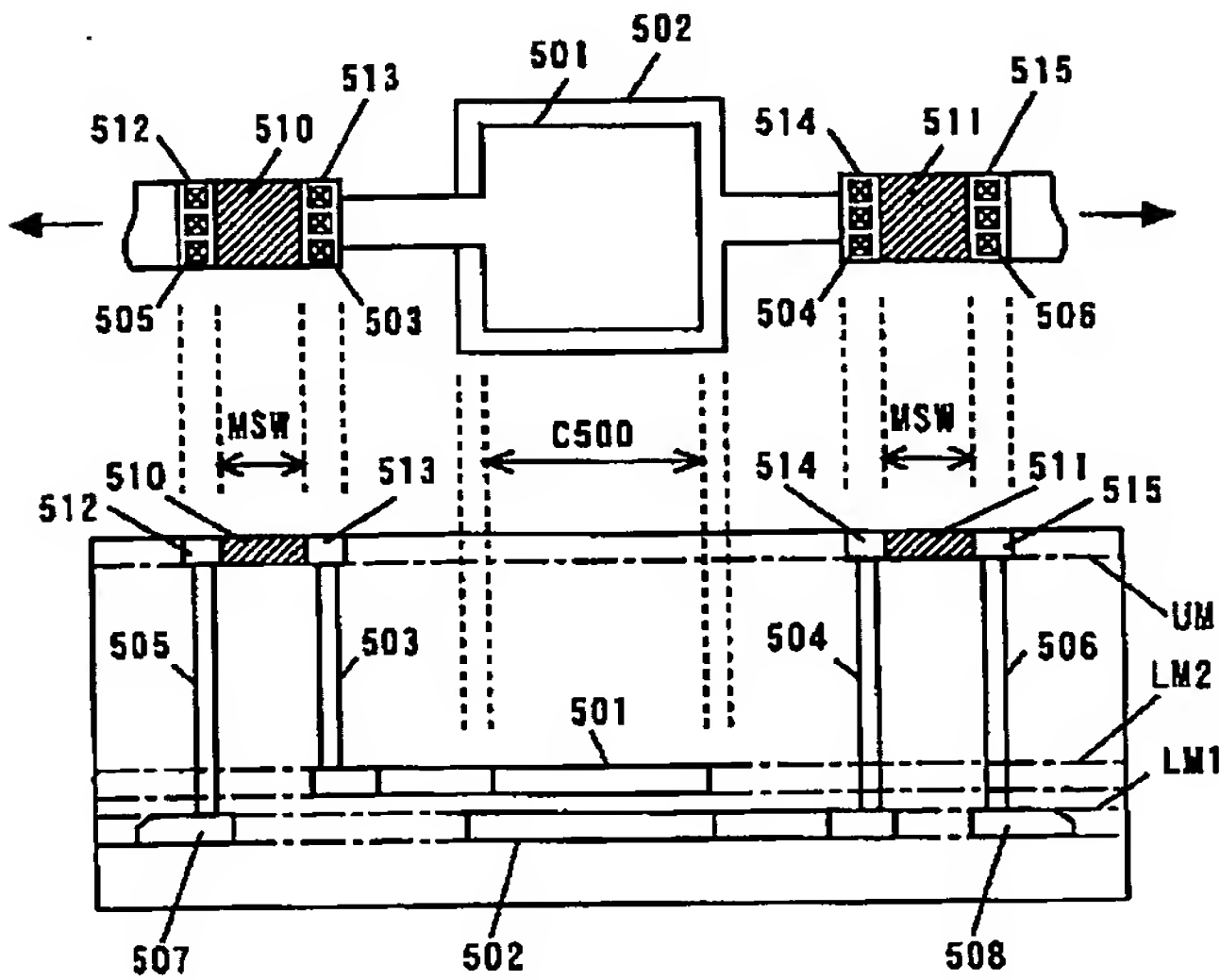
[Drawing 19]



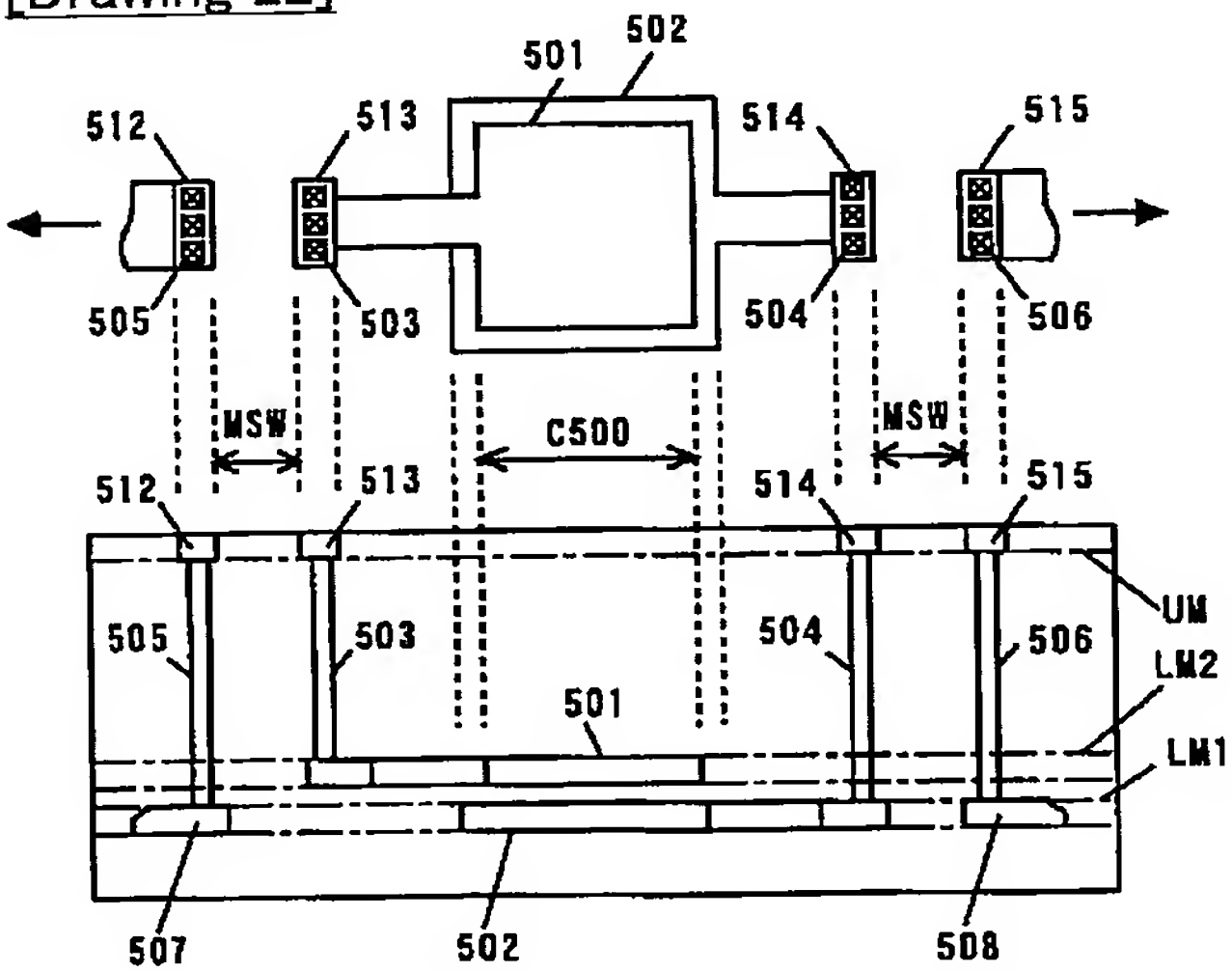
[Drawing 20]



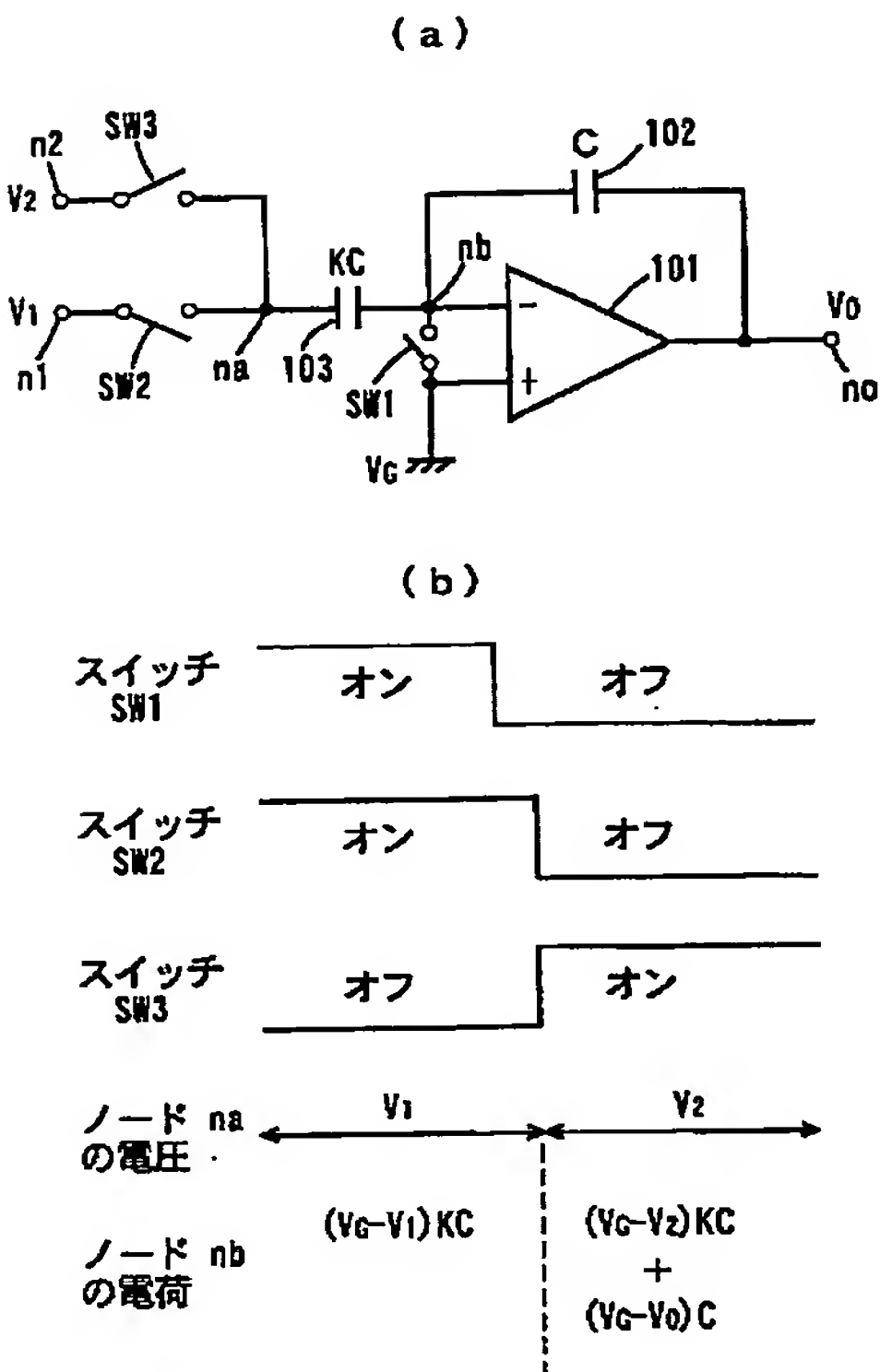
[Drawing 21]



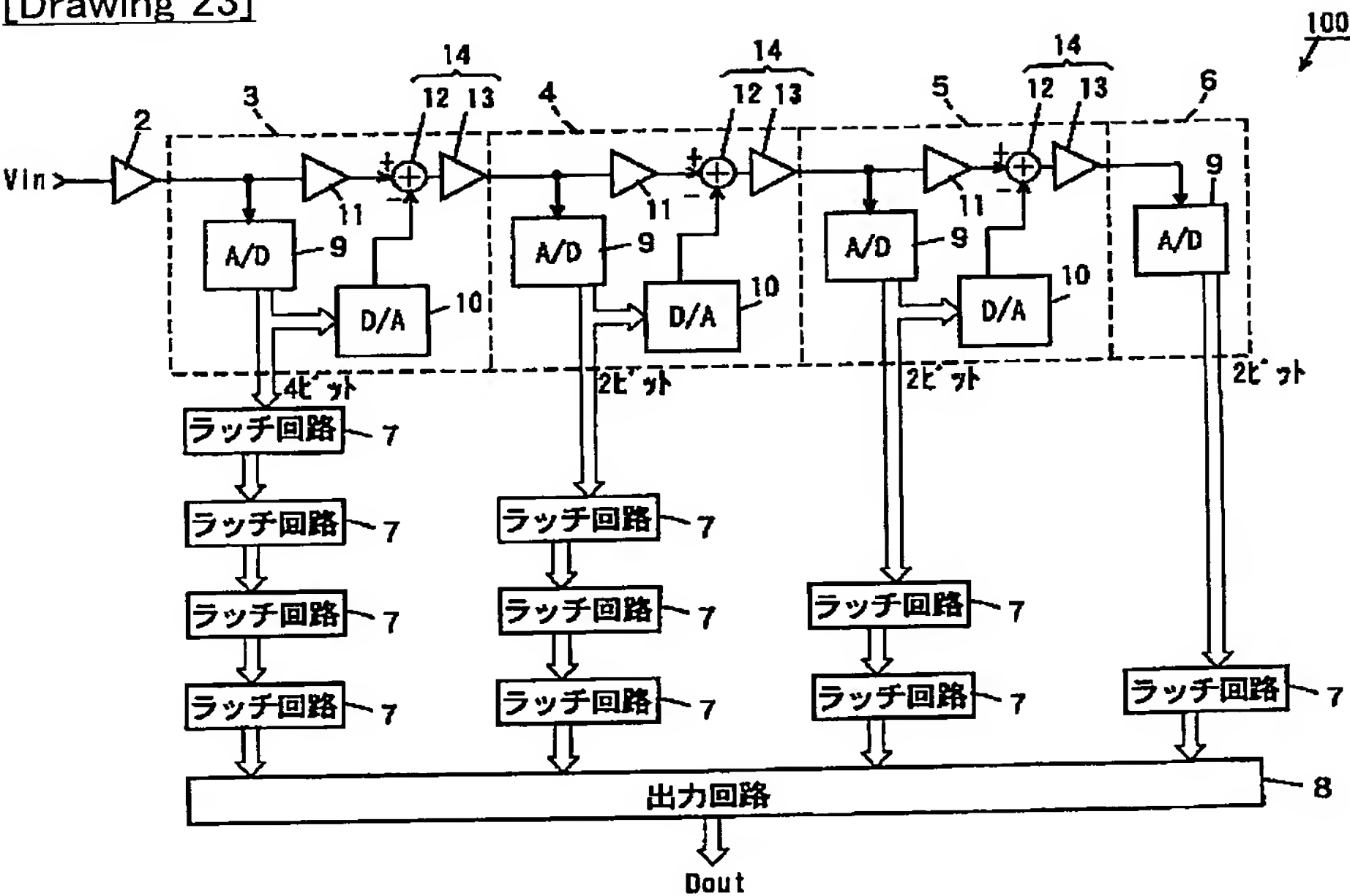
[Drawing 22]



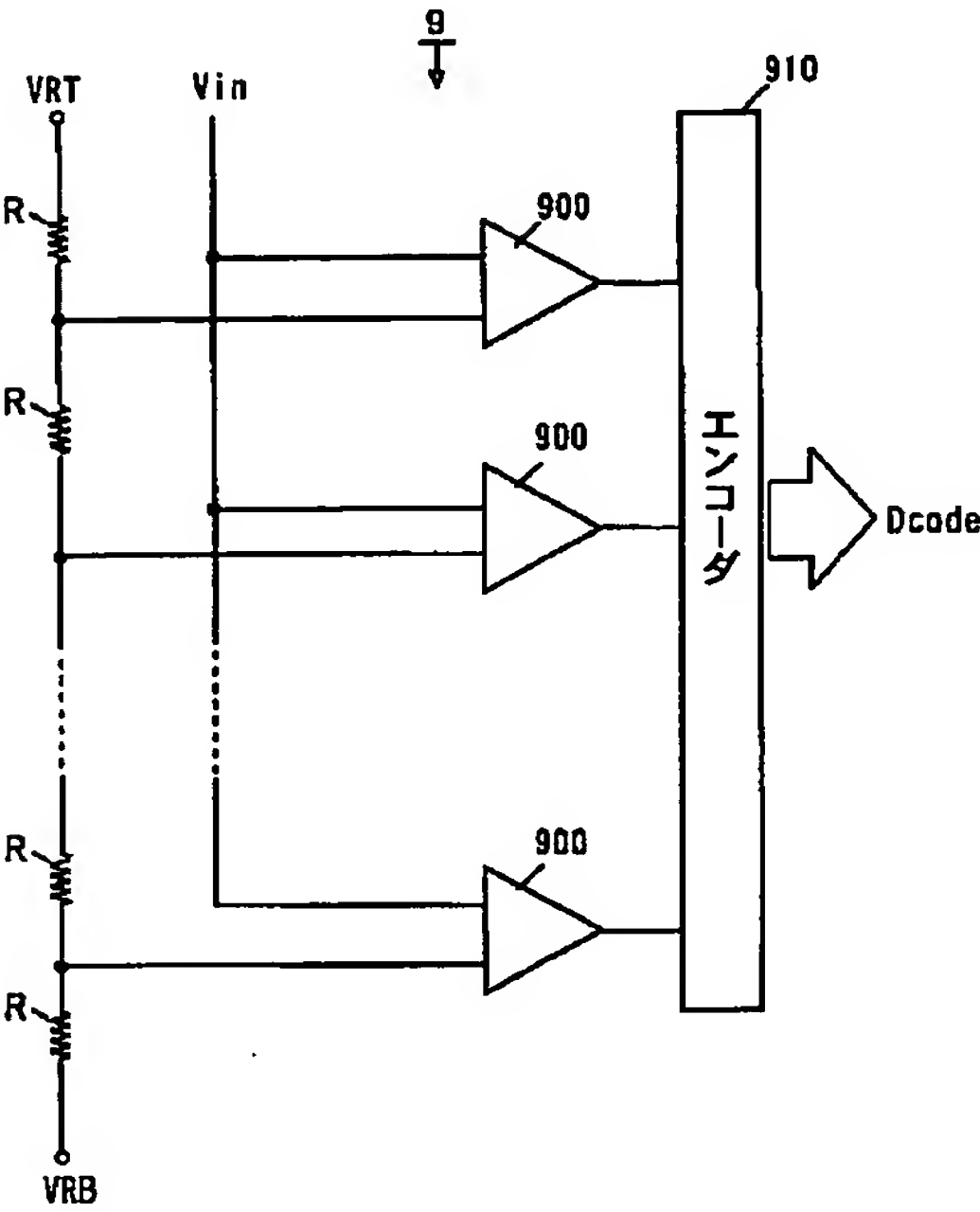
[Drawing 24]



[Drawing 23]

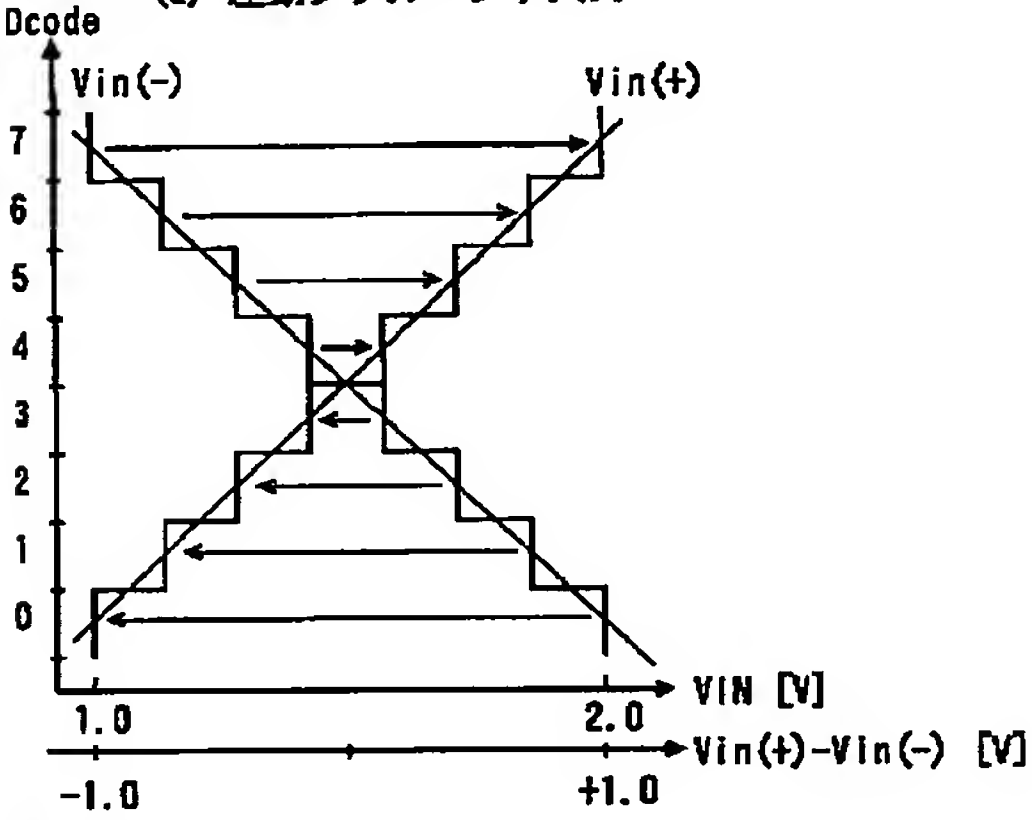


[Drawing 25]

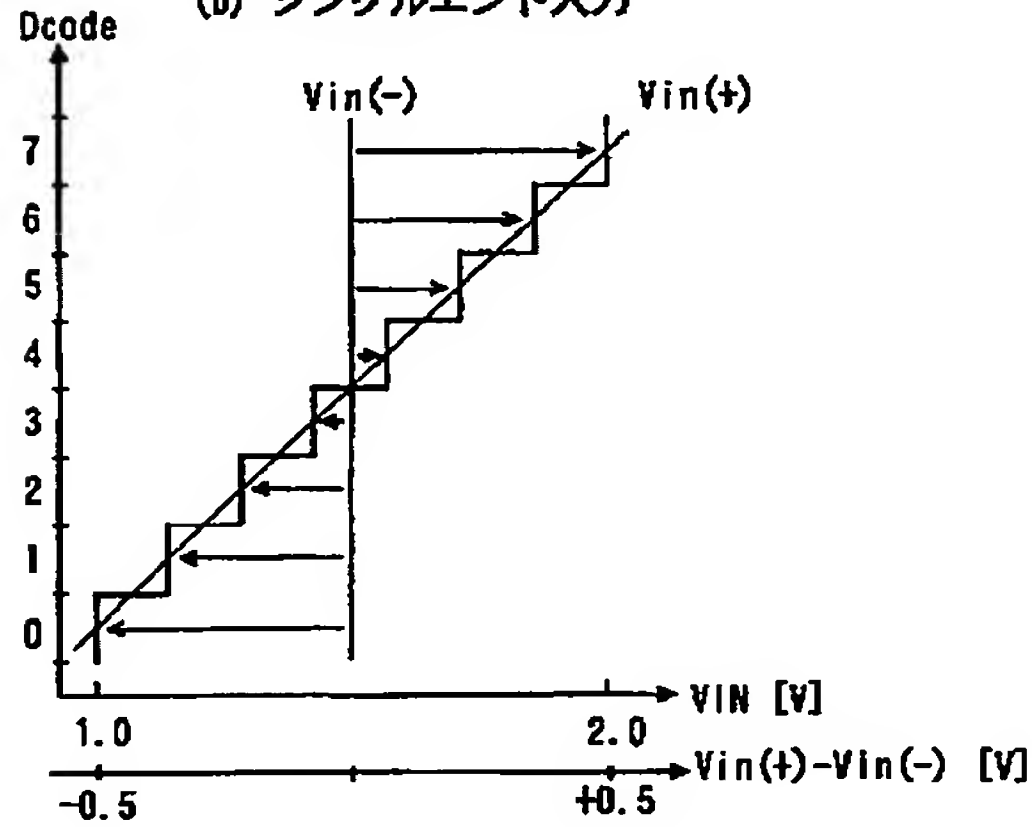


[Drawing 26]

(a) 差動ダブルエンド入力



(b) シングルエンド入力



[Translation done.]

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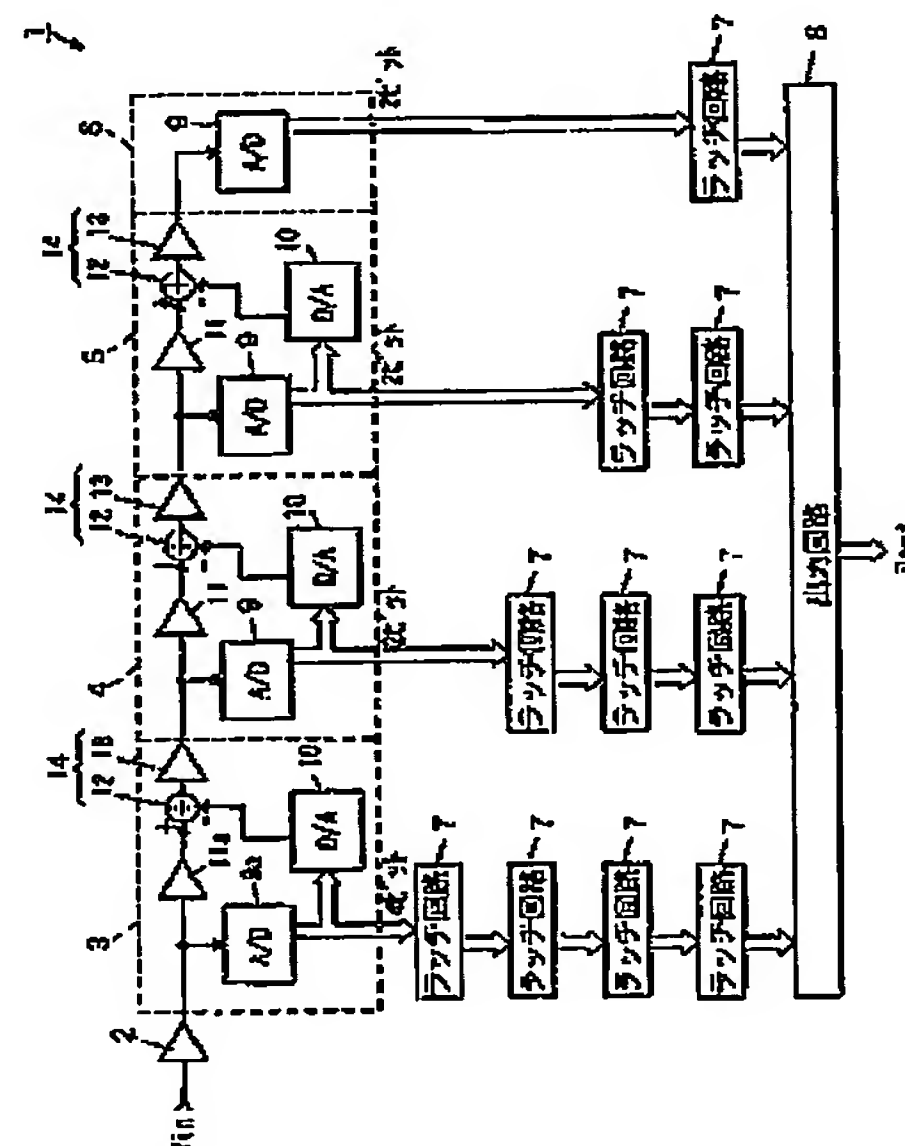
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(54) 【発明の名称】 アナログ-デジタル変換回路

(57) 【要約】

【課題】 回路構成の再設計を行うことなくアナログ入力信号の電圧レンジの変更または差動ダブルエンド入力とシングルエンド入力との間の入力方式の変更を容易に行うことができるパイプライン型アナログ-デジタル変換回路を提供することである。

【解決手段】 アナログ入力信号の電圧レンジが V_{IN_max} のときに、サブA/Dコンバータ9のフルスケールレンジは V_{IN_max} に切り替えられ、演算増幅回路11aの利得は1倍に切り替えられる。アナログ入力信号の電圧レンジが $V_{IN_max}/2$ のときに、サブA/Dコンバータ9のフルスケールレンジは $V_{IN_max}/2$ に切り替えられ、演算増幅回路11aの利得は2倍に切り替えられる。



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【特許請求の範囲】

【請求項1】 複数段の回路からなる多段パイプライン構成を有し、

最終段の回路を除く各段の回路は、

入力されたアナログ信号をデジタル信号に変換するアナログ-デジタル変換器と、

前記アナログ-デジタル変換器から出力されるデジタル信号をアナログ信号に変換するデジタル-アナログ変換器と、

入力されるアナログ信号と前記デジタル-アナログ変換器から出力されるアナログ信号との差分を増幅する第1の演算増幅回路とを備え、

最終段の回路は、入力されたアナログ信号をデジタル信号に変換するアナログ-デジタル変換器を含み、

最終段の回路を除く少なくとも1段の回路が、フルスケールレンジを複数段に切り替える切り替え手段を有するアナログ-デジタル変換器、フルスケールレンジを複数段に切り替える切り替え手段を有するデジタル-アナログ変換器および利得を複数段に切り替える切り替え手段を有する第1の演算増幅回路のうち少なくとも1つを含み、および/または最終段の回路がフルスケールレンジを複数段に切り替える切り替え手段を有するアナログ-デジタル変換器を含むことを特徴とするアナログ-デジタル変換回路。

【請求項2】 最終段の回路を除く各段の回路は、入力されたアナログ信号を増幅して前記第1の演算増幅回路に与える第2の演算増幅回路をさらに含み、最終段の回路を除く少なくとも1段の回路の前記第2の演算増幅回路は、利得を複数段に切り替える切り替え手段を有することを特徴とする請求項1記載のアナログ-デジタル変換回路。

【請求項3】 最終段の回路を除く少なくとも1段の回路の前記第1の演算増幅回路は、利得を複数段に切り替える切り替え手段を有することを特徴とする請求項1または2記載のアナログ-デジタル変換回路。

【請求項4】 少なくとも1段の回路の前記アナログ-デジタル変換器は、フルスケールレンジを複数段に切り替える切り替え手段を有することを特徴とする請求項1～3のいずれかに記載のアナログ-デジタル変換回路。

【請求項5】 最終段の回路を除く少なくとも1段の回路の前記デジタル-アナログ変換器は、フルスケールレンジを複数段に切り替える切り替え手段を有することを特徴とする請求項1～4のいずれかに記載のアナログ-デジタル変換回路。

【請求項6】 前記少なくとも1段の回路の前記第2の演算増幅回路は、入力容量、帰還容量および演算増幅器を有し、入力されたアナログ信号を前記入力容量の値および前記帰還容量の値により定まる利得で増幅し、

前記切り替え手段は、前記入力容量の値および前記帰還容量の値の少なくとも一方を可変に設定する可変部を含

むことを特徴とする請求項2記載のアナログ-デジタル変換回路。

【請求項7】 前記可変部は、前記入力容量または前記帰還容量の一部を切り離された状態または短絡された状態に切り替える切り替え部を含むことを特徴とする請求項6記載のアナログ-デジタル変換回路。

【請求項8】 前記少なくとも1段の回路の前記第1の演算増幅回路は、入力容量、帰還容量および演算増幅器を有し、入力されたアナログ信号を前記入力容量の値および前記帰還容量の値により定まる利得で増幅し、

前記切り替え手段は、前記入力容量の値および前記帰還容量の値の少なくとも一方を可変に設定する可変部を含むことを特徴とする請求項3記載のアナログ-デジタル変換回路。

【請求項9】 前記可変部は、前記入力容量または前記帰還容量の一部を切り離された状態または短絡された状態に切り替える切り替え部を含むことを特徴とする請求項8記載のアナログ-デジタル変換回路。

【請求項10】 前記帰還容量は、前記演算増幅器の入力端子と出力端子との間に並列または直列に設けられた第1および第2の容量を含み、前記切り替え部は、前記第2の容量に直列または並列に接続されたことを特徴とする請求項9記載のアナログ-デジタル変換回路。

【請求項11】 前記切り替え部は、前記演算増幅器の出力端子に接続されたことを特徴とする請求項10記載のアナログ-デジタル変換回路。

【請求項12】 前記入力容量は、前記演算増幅器の入力端子に並列または直列に設けられた第1および第2の容量を含み、前記切り替え部は、前記第2の容量に直列または並列に接続されたことを特徴とする請求項9記載のアナログ-デジタル変換回路。

【請求項13】 前記切り替え部は、前記第2の容量の入力側に接続されたことを特徴とする請求項12記載のアナログ-デジタル変換回路。

【請求項14】 少なくとも1段の回路の前記アナログ-デジタル変換器は、複数の基準電圧を発生する基準電圧発生回路と、前記基準電圧発生回路により発生された複数の基準電圧を入力されたアナログ信号と比較する複数の比較器とを含み、前記切り替え手段は、前記基準電圧発生回路により発生される複数の基準電圧を可変に設定する可変部を含むことを特徴とする請求項4記載のアナログ-デジタル変換回路。

【請求項15】 最終段の回路を除く少なくとも1段の回路の前記デジタル-アナログ変換器は、基準電圧を発生する基準電圧発生回路と、共通の端子に接続される複数の容量と、前記基準電圧発生回路と前記複数の容量との間に接続され、入力されるデジタル信号に応じて前記

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基準電圧発生回路により発生された基準電圧を前記複数の容量にそれぞれ与える複数のスイッチとを含み、前記切り替え手段は、前記基準電圧発生回路により発生される基準電圧を可変に設定する可変部を含むことを特徴とする請求項5記載のアナログーデジタル変換回路。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、多段パイプライン（ステップフラッシュ）構成を有するアナログーデジタル変換回路に関する。

【0002】

【従来の技術】近年、ビデオ信号のデジタル処理技術の進歩に伴い、ビデオ信号処理用のアナログーデジタル変換回路（A/Dコンバータ）の需要が大きくなっている。ビデオ信号処理用のアナログーデジタル変換回路には高速変換動作が要求されるため、従来、2ステップフラッシュ（2ステップパラレル）方式が広く用いられていた。

【0003】しかし、変換ビット数の増大に伴い、2ステップフラッシュ方式では十分な変換精度が得られなくなってきたため、多段パイプライン（ステップフラッシュ）構成を有するアナログーデジタル変換回路が開発された。

【0004】図23は特開平11-88172号公報に開示された従来のアナログーデジタル変換回路を示すブロック図である。図23のアナログーデジタル変換回路100は、10ビット4段パイプライン構成を有する。

【0005】図23において、アナログーデジタル変換回路100は、サンプルホールド回路2、1段目～4段目の回路3～6、複数のラッチ回路7および出力回路8から構成されている。

【0006】1段目（初段）～3段目の回路3、4、5は、サブA/Dコンバータ9、D/Aコンバータ10、演算増幅回路11、減算回路12および演算増幅回路13を備える。減算回路12および演算増幅回路13が減算増幅回路14を構成する。1段目の回路3内の演算増幅回路11の利得は1であり、1段目の回路3内の演算増幅回路13および2段目および3段目の回路4、5内の演算増幅回路11、13の利得は2である。4段目

（最終段）の回路6は、サブA/Dコンバータ9のみを*

*倍える。

【0007】1段目の回路3は4ビット構成、2～4段目の回路4～6はそれぞれ2ビット構成である。1～3段目の回路3～5において、サブA/Dコンバータ9およびD/Aコンバータ10のビット数（ビット構成）は同じに設定されている。

【0008】

【発明が解決しようとする課題】ここで、上記のアナログーデジタル変換回路100では、アナログ入力信号 V_{in} の電圧レンジを $V_{IN..}$ とすると、1段目の回路3内のサブA/Dコンバータ9のフルスケールレンジはアナログ入力信号の電圧レンジ $V_{IN..}$ と等しい。2～4段目の回路4～6内のサブA/Dコンバータ9のフルスケールレンジはそれぞれ1～3段目の回路3～5の減算増幅回路14の出力電圧レンジ $V_{IN..}/8$ と等しい。

【0009】また、1段目の回路3内のD/Aコンバータ10のフルスケールレンジはサブA/Dコンバータ9と同様にアナログ入力信号 V_{in} の電圧レンジ $V_{IN..}$ と等しい。2段目および3段目の回路4、5内のD/Aコンバータ10の電圧のフルスケールレンジは利得2を有する演算増幅回路11の出力電圧レンジとの整合を取るためにサブA/Dコンバータ9のフルスケールレンジの2倍の $V_{IN..}/4$ となる。

【0010】次に、図23のアナログーデジタル変換回路1の動作を説明する。サンプルホールド回路2は、アナログ入力信号 V_{in} をサンプリングして一定時間保持する。サンプルホールド回路2から出力されたアナログ入力信号 V_{in} は、1段目の回路3へ転送される。

【0011】1段目の回路3において、サブA/Dコンバータ9は、電圧レンジ $V_{IN..}$ のアナログ入力信号 V_{in} に対してアナログーデジタル変換を行う。ここで、サブA/Dコンバータ9のフルスケールレンジは、上記のように $V_{IN..}$ である。サブA/Dコンバータ9のアナログーデジタル変換結果であるデジタル出力（ 2^3 、 2^4 、 2^5 、 2^6 ）は、D/Aコンバータ10へ転送されるとともに、4つのラッチ回路7を介して出力回路8へ転送される。D/Aコンバータ10の正規出力電圧レンジは、次式のように表される。

【0012】

$$\begin{aligned} & (1 \text{ 段目の分解能} - 1) \times (D/A \text{ コンバータ } 10 \text{ のフルスケールレンジ}) / \\ & (1 \text{ 段目の分解能}) \\ & = (2^4 - 1) \times (V_{IN..}) / 2^4 \\ & = 15 V_{IN..} / 16 \end{aligned}$$

一方、演算増幅回路11は、アナログ入力信号 V_{in} をサンプリングして増幅および保持する。演算増幅回路11*

*1の出力電圧レンジは、次式のように表される。

【0013】

$$\begin{aligned} & (アナログ入力信号 V_{in} の電圧レンジ $V_{IN..}$) \times (演算増幅回路 11 の \\ & 利得) \\ & = V_{IN..} \times 1 \\ & = V_{IN..} \end{aligned}$$

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減算増幅回路14は、演算増幅回路11から出力されたアナログ入力信号 V_{in} とD/Aコンバータ10のD/A変換結果とを減算して増幅する。減算増幅回路14の出力は、2段目の回路4へ転送される。1段目の減算*

*増幅回路14の出力電圧レンジは、次式のように表される。

【0014】

$$\begin{aligned} & ((\text{演算増幅回路11の出力電圧レンジ}) - (\text{D/Aコンバータ10の正規出力電圧レンジ})) \times (\text{減算増幅回路14の利得}) \\ &= ((V_{IN_{max}}) - (15V_{IN_{max}}/16)) \times 2 \\ &= V_{IN_{max}}/8 \end{aligned}$$

2段目の回路4においては、サブA/Dコンバータ9が、1段目の回路3の減算増幅回路14の出力に対してA/D変換を行う。サブA/Dコンバータ9のA/D変換結果は、D/Aコンバータ10へ転送されるとともに、3つのラッチ回路7を介して出力回路8へ転送され*

る。これにより、2段目の回路4から中上位2ビットのデジタル出力(2', 2'')が得られる。D/Aコンバータ10の正規出力電圧レンジは、次式のように表される。

【0015】

$$\begin{aligned} & ((2\text{段目の分解能}-1) \times (\text{D/Aコンバータ10のフルスケールレンジ}) / \\ & (2\text{段目の分解能})) \\ &= (2^2-1) \times (V_{IN_{max}}/4) / 2^2 \\ &= 3V_{IN_{max}}/16 \end{aligned}$$

一方、演算増幅回路11は、1段目の回路3の演算増幅回路13の出力を増幅する。演算増幅回路11の出力電*

★圧レンジは次式のように表される。

【0016】

$$\begin{aligned} & ((1\text{段目の減算増幅回路14の出力電圧レンジ}) \times (\text{演算増幅回路11の利得})) \\ &= (V_{IN_{max}}/8) \times 2 \\ &= V_{IN_{max}}/4 \end{aligned}$$

減算増幅回路14は、演算増幅回路11の出力とD/Aコンバータ10のD/A変換結果とを減算して増幅する。減算増幅回路14の出力は、3段目の回路5へ転送*

☆される。2段目の減算増幅回路14の出力電圧のレンジは、次式のように表される。

【0017】

$$\begin{aligned} & ((\text{演算増幅回路11の出力電圧レンジ}) - (\text{D/Aコンバータ10の正規出力電圧レンジ})) \times (\text{減算増幅回路14の利得}) \\ &= ((V_{IN_{max}}/4) - (3V_{IN_{max}}/16)) \times 2 \\ &= V_{IN_{max}}/8 \end{aligned}$$

3段目の回路5においては、2段目の回路3の演算増幅回路14の出力に対して2段目の回路4と同様の動作が行われる。それにより、3段目の回路5から中下位2ビットのデジタル出力(2', 2'')が得られる。各部の出力電圧レンジは2段目の回路4と同様である。

【0018】4段目の回路6においては、3段目の回路5の演算増幅回路14の出力に対してサブA/Dコンバータ9がA/D変換を行い、下位2ビットのデジタル出力(2', 2'')が得られる。

【0019】1段目～4段目の回路3～6のデジタル出力は、各ラッチ回路7を経て同時に出力回路8に到達する。すなわち、各ラッチ回路7は各回路3～6のデジタル出力の同期をとるために設けられている。

【0020】出力回路8は、アナログ入力信号 V_{in} の10ビットのデジタル出力 D_{out} を必要場合はデジタル補正処理後パラレル出力する。

【0021】このようにして、変換ビット数が増大し、電源電圧の減少に伴いLSB(Least Significant Bit)が小さくなっても、サブA/Dコンバータ9の分解能を向上させることができ、十分な変換精度が得られ

る。

【0022】図24(a)は図23のアナログ-デジタル変換回路の減算増幅回路の構成を示す回路図。図24(b)は図24(a)の減算増幅回路の動作を説明するための図である。

【0023】図24において、演算増幅器101の反転入力端子はノードn1に接続され、非反転入力端子は接地されている。また、演算増幅器101の出力端子はノードn0に接続されるとともにコンデンサ102を介して反転入力端子に接続されている。演算増幅器1の反転入力端子と非反転入力端子との間にはスイッチSW1が接続され、ノードn1とノードnaとの間にコンデンサ103が接続されている。ノードnaは、スイッチSW2を介してノードn1に接続され、かつスイッチSW3を介してノードn2に接続されている。これらのスイッチSW2、SW3は、通常CMOS(相補型金属酸化物半導体)電界効果トランジスタからなるCMOSスイッチにより構成される。

【0024】ノードn1に電圧 V_1 が入力され、ノードn2に電圧 V_2 が入力され、ノードn0から電圧 V_0 が

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出力される。

【0025】ここで、図24(b)を参照しながら図24(a)の減算増幅回路の動作を説明する。なお、コンデンサ101の容量値をCとし、コンデンサ103の容量値をKCとし、接地電位をV_cとする。Kは定数である。

【0026】まず、スイッチSW1およびスイッチSW2をオンにし、スイッチSW3をオフにする。それにより、ノードnaの電圧はV₁となる。また、ノードnoの電圧は0となる。このとき、ノードnbの電荷Q_aは

$$Q_a = (V_c - V_1) KC$$

次に、スイッチSW1をオフにした後、スイッチSW2をオフにし、かつスイッチSW3をオンにする。それにより、ノードnaの電圧はV₂となる。また、ノードnoの電圧はV₂となる。このとき、ノードnbは仮想接地するため、ノードnbの電荷Q_bは次式のようになる。

$$Q_b = (V_c - V_2) KC + (V_c - V_1) C$$

ノードnbには電荷が抜け出る経路がないので、電荷保存則によりQ_a = Q_bとなる。したがって、次式が成立する。

$$(V_c - V_1) KC = (V_c - V_2) KC + (V_c - V_1) C$$

上式から、ノードnoの電圧V₂は次式のようになる。

$$V_2 = V_1 + (V_1 - V_c) K$$

このようにして、電圧V₁から電圧V₂が減算され、その減算値がK倍に増幅される。

【0031】したがって、減算増幅回路は電圧V₁と電圧V₂との差をコンデンサ103とコンデンサ102との容量比で決まる利得によって出力する機能を有する。例えば、KC = C (K = 1) に設定することにより、減算増幅回路に利得1倍のサンプルホールド機能を持たせることとなる。

【0032】図25は図23のアナログーデジタル変換回路において用いられるサブA/Dコンバータの構成を示す図である。

【0033】図25の並列型アナログーデジタルコンバータ9においては、複数のコンパレータ900が配置されている。複数のコンパレータ900の一方の入力端子にはアナログ入力電圧V_{in}が与えられ、他方の入力端子には高電位側基準電圧V_{RT}と低電位側基準電圧V_{RB}との間の電圧を複数の抵抗Rで分圧することにより得られる基準電圧がそれぞれ与えられる。各コンパレータ900は、一方の入力端子の電圧と他方の入力端子の電圧とを比較する。複数のコンパレータ900の比較結果をエンコーダ910によってエンコードすることにより、デジタルコードD_{code}を得ることができる。

【0034】ところで、アナログーデジタル変換回路に

与えるアナログ入力信号の電圧レンジを変更する場合、またはアナログーデジタル変換回路に与えるアナログ入力信号の方式を差動ダブルエンド入力とシングルエンド入力とで変更する場合には、アナログーデジタル変換回路の仕様を変更する必要がある。

【0035】ここで、差動ダブルエンド入力およびシングルエンド入力について説明する。図26(a)、

(b)は差動ダブルエンド入力およびシングルエンド入力におけるアナログーデジタル変換を説明するための図である。横軸はアナログ入力電圧V_{in}を示し、縦軸は出力されたデジタルコードD_{code}を示す。

【0036】図26(a)に示すように、差動ダブルエンド入力時においては、アナログ入力信号V_{in}の正側アナログ入力電圧V_{in}(+)および負側アナログ入力電圧V_{in}(-)が相対的に変化する。それにより、正側アナログ入力電圧V_{in}(+)と負側アナログ入力電圧V_{in}(-)との差分がアナログ入力信号V_{in}の電圧レンジV_{IN_{max}}となる。

【0037】したがって、図26(a)に示すように、正側アナログ入力電圧V_{in}(+)が1.0Vから2.0Vの範囲で変化し、負側アナログ入力電圧V_{in}(-)が2.0Vから1.0Vの範囲で変化する場合、アナログ入力信号V_{in}の電圧レンジはV_{in}(+) - V_{in}(-)の演算から2.0Vとなる。

【0038】一方、図26(b)に示すように、シングルエンド入力時においては、正側アナログ入力電圧V_{in}(+)のみが変化する。それにより、正側アナログ入力電圧V_{in}(+)の電圧レンジがアナログ入力信号V_{in}の電圧レンジとなる。

【0039】したがって、図26(b)に示すように、正側アナログ入力電圧V_{in}(+)が1.0Vから2.0Vの範囲で変化する場合、アナログ入力信号の電圧レンジは1.0Vとなる。

【0040】すなわち、差動ダブルエンド入力方式のアナログ入力信号V_{in}の電圧レンジを2V_{IN_{max}}とすると、シングルエンド入力方式のアナログ入力信号V_{in}の電圧レンジはV_{IN_{max}}となる。

【0041】このように、差動ダブルエンド入力方式とシングルエンド入力方式とでは、各アナログ入力電圧の変化の範囲が同じであっても、アナログ入力信号の電圧レンジが異なることになる。

【0042】上記の従来のアナログーデジタル変換回路では、アナログ入力信号の電圧レンジの変更を行う場合、またはアナログ入力信号の入力方式の変更を行う場合に、回路構成を再設計する必要がある。

【0043】本発明の目的は、回路構成の再設計を行うことなくアナログ入力信号の電圧レンジの変更または差動ダブルエンド入力とシングルエンド入力との間の入力方式の変更を容易に行うことができるバイブライン型アナログーデジタル変換回路を提供することである。

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【0044】

【課題を解決するための手段および発明の効果】(1)

第1の発明

第1の発明に係るアナログ-デジタル変換回路は、複数段の回路からなる多段パイプライン構成を有し、最終段の回路を除く各段の回路は、入力されたアナログ信号をデジタル信号に変換するアナログ-デジタル変換器と、アナログ-デジタル変換器から出力されるデジタル信号をアナログ信号に変換するデジタル-アナログ変換器と、入力されるアナログ信号とデジタル-アナログ変換器から出力されるアナログ信号との差分を増幅する第1の演算増幅回路とを備え、最終段の回路は、入力されたアナログ信号をデジタル信号に変換するアナログ-デジタル変換器を含み、最終段の回路を除く少なくとも1段の回路が、フルスケールレンジを複数段に切り替える切り替え手段を有するアナログ-デジタル変換器、フルスケールレンジを複数段に切り替える切り替え手段を有するデジタル-アナログ変換器および利得を複数段に切り替える切り替え手段を有する第1の演算増幅回路のうち少なくとも1つを含み、および/または最終段の回路がフルスケールレンジを複数段に切り替える切り替え手段を有するアナログ-デジタル変換器を含むものである。

【0045】本発明に係るアナログ-デジタル変換回路においては、最終段の回路を除く少なくとも1段の回路が、フルスケールレンジを複数段に切り替える切り替え手段を有するアナログ-デジタル変換器、フルスケールレンジを複数段に切り替える切り替える切り替え手段を有するデジタル-アナログ変換器および利得を複数段に切り替える切り替え手段を有する第1の演算増幅回路のうち少なくとも1つを含み、および/または最終段の回路がフルスケールレンジを複数段に切り替える切り替え手段を有するアナログ-デジタル変換器を含むので、アナログ-デジタル変換回路のフルスケールレンジ、デジタル-アナログ変換器のフルスケールレンジおよび第1の演算増幅回路の利得のうち少なくとも1つを切り替えることができる。

【0046】それにより、差動ダブルエンド入力方式をシングルエンド入力方式に変更することによりアナログ入力信号の電圧レンジが変更されても、回路構成の再設計が不要となる。また、シングルエンド入力のアナログ入力信号の電圧レンジを変更する場合または差動ダブルエンド入力のアナログ入力信号の電圧レンジを変更する場合にも、回路構成の再設計が不要となる。

【0047】したがって、回路構成の再設計を行うことなくアナログ入力信号の電圧レンジの変更または差動ダブルエンド入力とシングルエンド入力との間の入力方式の変更を容易に行うことができる。

【0048】その結果、アナログ-デジタル変換回路の開発期間の短縮化を図ることができるとともに、電圧レンジの最適化を最適化することにより低消費電力化を容

易に行うことができる。

【0049】(2)第2の発明

第2の発明に係るアナログ-デジタル変換回路は、第1の発明に係るアナログ-デジタル変換回路の構成において、最終段の回路を除く各段の回路は、入力されたアナログ信号を増幅して第1の演算増幅回路に与える第2の演算増幅回路をさらに含み、最終段の回路を除く少なくとも1段の回路の第2の演算増幅回路は、利得を複数段に切り替える切り替え手段を有するものである。

10 【0050】この場合、少なくとも1段の回路の第2の演算増幅回路の利得を複数段に切り替えることにより、回路構成の再設計を行うことなくアナログ入力信号の電圧レンジの変更または差動ダブルエンド入力とシングルエンド入力との間の入力方式の変更を容易に行うことが可能となる。

【0051】(3)第3の発明

第3の発明に係るアナログ-デジタル変換回路は、第1または第2の発明に係るアナログ-デジタル変換回路の構成において、最終段の回路を除く少なくとも1段の回路の第1の演算増幅回路は、利得を複数段に切り替える切り替え手段を有するものである。

20 【0052】この場合、少なくとも1段の回路の第1の演算増幅回路の利得を複数段に切り替えることにより、回路構成の再設計を行うことなくアナログ入力信号の電圧レンジの変更または差動ダブルエンド入力とシングルエンド入力との間の入力方式の変更を容易に行うことが可能となる。

【0053】(4)第4の発明

第4の発明に係るアナログ-デジタル変換回路は、第1〜第3のいずれかの発明に係るアナログ-デジタル変換回路の構成において、少なくとも1段の回路のアナログ-デジタル変換器は、フルスケールレンジを複数段に切り替える切り替え手段を有するものである。

30 【0054】この場合、少なくとも1段の回路のアナログ-デジタル変換器のフルスケールレンジを複数段に切り替え可能ることにより、回路構成の再設計を行うことなくアナログ入力信号の電圧レンジの変更または差動ダブルエンド入力とシングルエンド入力との間の入力方式の変更を容易に行うことが可能となる。

40 【0055】(5)第5の発明

第5の発明に係るアナログ-デジタル変換回路は、第1〜第4のいずれかの発明に係るアナログ-デジタル変換回路の構成において、最終段の回路を除く少なくとも1段の回路のデジタル-アナログ変換器は、フルスケールレンジを複数段に切り替える切り替え手段を有するものである。

50 【0056】この場合、少なくとも1段の回路のデジタル-アナログ変換器のフルスケールレンジを複数段に切り替えることにより、回路構成の再設計を行うことなくアナログ入力信号の電圧レンジの変更または差動ダブル

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エンド入力とシングルエンド入力との間の入力方式の変更を容易に行うことが可能となる。

【0057】(6)第6の発明

第6の発明に係るアナログ-デジタル変換回路は、第2の発明に係るアナログ-デジタル変換回路の構成において、少なくとも1段の回路の第2の演算増幅回路は、入力容量、帰還容量および演算増幅器を有し、入力されたアナログ信号を入力容量の値および帰還容量の値により定まる利得で増幅し、切り替え手段は、入力容量の値および帰還容量の値の少なくとも一方を可変に設定する可変部を含むものである。

【0058】この場合、入力されたアナログ信号が入力容量の値および帰還容量の値により定まる利得で増幅される。したがって、演算増幅器の入力容量の値および帰還容量の値の少なくとも一方を変更することにより、第2の演算増幅回路の利得を容易に切り替えることができる。

【0059】(7)第7の発明

第7の発明に係るアナログ-デジタル変換回路は、第6の発明に係るアナログ-デジタル変換回路の構成において、可変部は、入力容量または帰還容量の一部を切り離された状態または短絡された状態に切り替える切り替え部を含むものである。

【0060】この場合、切り替え部により入力容量または帰還容量の一部を切り離された状態または短絡された状態に切り替えることにより、演算増幅器の入力容量または帰還容量を変更することができる。それにより、第2の演算増幅回路の利得を容易に切り替えることができる。

【0061】(8)第8の発明

第8の発明に係るアナログ-デジタル変換回路は、第3の発明に係るアナログ-デジタル変換回路の構成において、少なくとも1段の回路の第1の演算増幅回路は、入力容量、帰還容量および演算増幅器を有し、入力されたアナログ信号を入力容量の値および帰還容量の値により定まる利得で増幅し、切り替え手段は、入力容量の値および帰還容量の値の少なくとも一方を可変に設定する可変部を含むものである。

【0062】この場合、入力されたアナログ信号が入力容量の値および帰還容量の値により定まる利得で増幅される。したがって、演算増幅器の入力容量の値および帰還容量の値の少なくとも一方を変更することにより、第1の演算増幅回路の利得を容易に切り替えることができる。

【0063】(9)第9の発明

第9の発明に係るアナログ-デジタル変換回路は、第8の発明に係るアナログ-デジタル変換回路の構成において、可変部は、入力容量または帰還容量の一部を切り離された状態または短絡された状態に切り替える切り替え部を含むものである。

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【0064】この場合、切り替え部により入力容量または帰還容量の一部を切り離された状態または短絡された状態に切り替えることにより、演算増幅器の入力容量または帰還容量を変更することができる。それにより、第1の演算増幅回路の利得を容易に切り替えることができる。

【0065】(10)第10の発明

第10の発明に係るアナログ-デジタル変換回路は、第9の発明に係るアナログ-デジタル変換回路の構成において、帰還容量は、演算増幅器の入力端子と出力端子との間に並列または直列に設けられた第1および第2の容量を含み、切り替え部は、第2の容量に直列または並列に接続されたものである。

【0066】切り替え部を接続状態にすると、演算増幅器の入力端子と出力端子との間に第1および第2の容量が並列または直列に接続される。それにより、帰還容量が増加または減少する。また、切り替え部を遮断状態にすると、演算増幅器の入力端子と出力端子との間に第1の容量のみが接続される。それにより、帰還容量が減少または増加する。

【0067】(11)第11の発明

第11の発明に係るアナログ-デジタル変換回路は、第10の発明に係るアナログ-デジタル変換回路の構成において、切り替え部は、演算増幅器の出力端子に接続されたものである。

【0068】第2の容量が切り替え部よりも出力側に接続されている場合、切り替え部が遮断状態に設定されても、第2の容量の寄生容量が充電される。それにより、利得の設定時に、寄生容量を考慮する必要性が生じ、寄生容量のばらつきにより利得がばらつくことになる。ここでは、切り替え部が第2の容量よりも出力側に接続されることにより、切り替え部が遮断状態に設定された場合に切り替え部により第2の容量が出力端子から寄生容量とともに切り離される。したがって、利得の設定時に第2の容量の寄生容量を考慮する必要がなくなり、寄生容量のばらつきによる利得のばらつきがなくなる。

【0069】(12)第12の発明

第12の発明に係るアナログ-デジタル変換回路は、第9の発明に係るアナログ-デジタル変換回路の構成において、入力容量は、演算増幅器の入力端子に並列または直列に設けられたものである。

【0070】切り替え部を接続状態にすると、演算増幅器の入力端子に第1および第2の容量が並列または直列に接続される。それにより、入力容量が増加または減少する。また、切り替え部を遮断状態にすると、演算増幅器の入力端子に第1の容量のみが接続される。それにより、入力容量が減少または増加する。

【0071】(13)第13の発明

第13の発明に係るアナログ-デジタル変換回路は、第12の発明に係るアナログ-デジタル変換回路の構成に

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において、切り替え部は、第2の容量の入力側に接続されたものである。

【0072】第2の容量が切り替え部よりも入力側に接続されている場合、切り替え部が遮断状態に設定されても、第2の容量の寄生容量が充電される。それにより、利得の設定時に、寄生容量を考慮する必要が生じ、寄生容量のばらつきにより利得がばらつくことになる。ここでは、切り替え部が第2の容量よりも入力側に接続されることにより、切り替え部が遮断状態に設定された場合に切り替え部により第2の容量が入力信号を受けるノードから寄生容量とともに切り離される。したがって、利得の設定時に第2の容量の寄生容量を考慮する必要がなくなり、寄生容量のばらつきによる利得のばらつきがなくなる。

【0073】(14)第14の発明

第14の発明に係るアナログ-デジタル変換回路は、第4の発明に係るアナログ-デジタル変換回路の構成において、少なくとも1段の回路のアナログ-デジタル変換器は、複数の基準電圧を発生する基準電圧発生回路と、基準電圧発生回路により発生された複数の基準電圧を入力されたアナログ信号と比較する複数の比較器とを含み、切り替え手段は、基準電圧発生回路により発生される複数の基準電圧を可変に設定する可変部を含むものである。

【0074】この場合、基準電圧発生回路により発生される基準電圧を変更することにより、基準電圧の電圧レンジを変更することができる。それにより、アナログ-デジタル変換器のフルスケールレンジを容易に切り替えることができる。

【0075】(15)第15の発明

第15の発明に係るアナログ-デジタル変換回路は、第5の発明に係るアナログ-デジタル変換回路の構成において、最終段の回路を除く少なくとも1段の回路のデジタル-アナログ変換器は、基準電圧を発生する基準電圧発生回路と、共通の端子に接続される複数の容量と、基準電圧発生回路と複数の容量との間に接続され、入力されるデジタル信号に応じて基準電圧発生回路により発生された基準電圧を複数の容量にそれぞれ与える複数のスイッチとを含み、切り替え手段は、基準電圧発生回路により発生される基準電圧を可変に設定する可変部を含むものである。

【0076】この場合、基準電圧発生回路により発生される基準電圧を変更することにより、基準電圧の電圧レンジを変更することができる。それにより、デジタル-アナログ変換器のフルスケールレンジを容易に切り替えることができる。

【0077】

【発明の実施の形態】(1)第1の実施の形態

図1は本発明の第1の実施の形態におけるパイプライン型アナログ-デジタル変換回路の構成を示すブロック図

である。図1のアナログ-デジタル変換回路は、10ビット4段パイプライン構成を有する。

【0078】図1において、アナログ-デジタル変換回路1は、サンプルホールド回路2、1段目～4段目の回路3～6、複数のラッチ回路7および出力回路8から構成されている。

【0079】1段目(初段)の回路3は、切り替え可能なフルスケールレンジを有するサブA/Dコンバータ9a、D/Aコンバータ10、切り替え可能な利得を有する演算増幅回路11a、減算回路12および演算増幅回路13を備える。減算回路12および演算増幅回路13が減算増幅回路14を構成する。2段目および3段目の回路4、5は、サブA/Dコンバータ9、D/Aコンバータ10、演算増幅回路11、減算回路12および演算増幅回路13を備える。減算回路12および演算増幅回路13が減算増幅回路14を構成する。4段目(最終段)の回路6は、サブA/Dコンバータ9のみを備える。

【0080】図1のパイプライン型アナログ-デジタル変換回路1が図20の従来のアナログ-デジタル変換回路100と異なるのは、1段目の回路3に切り替え可能なフルスケールレンジを有するサブA/Dコンバータ9aおよび切り替え可能な利得を有する演算増幅回路11aが用いられる点である。

【0081】ここでは、1段目の回路3内のサブA/Dコンバータ9のフルスケールレンジは、アナログ入力信号の電圧レンジが $V_{IN_}$ のときに、それと等しい電圧レンジ $V_{IN_}$ に切り替えられ、アナログ入力信号の電圧レンジが $V_{IN_}/2$ のときには、それと等しい電圧レンジ $V_{IN_}/2$ に切り替えられる。また、1段目の回路3内の演算増幅回路11aの利得は、アナログ入力信号の電圧レンジが $V_{IN_}$ のときには1倍に切り替えられ、アナログ入力信号の電圧レンジが $V_{IN_}/2$ のときには2倍に切り替えられる。

【0082】1段目～3段目の回路3～5内のD/Aコンバータ10のフルスケールレンジは固定され、2段目～4段目の回路4～6内のサブA/Dコンバータ9のフルスケールレンジは固定されている。また、1段目の回路3内の演算増幅回路13および2段目および3段目の回路3、4内の演算増幅回路11、13の利得は2である。

【0083】1段目の回路3は4ビット構成、2～4段目の回路4～6はそれぞれ2ビット構成である。1～3段目の回路3～5において、サブA/Dコンバータ9、9aおよびD/Aコンバータ10のビット数(ビット構成)は同じに設定されている。

【0084】アナログ入力信号の電圧レンジが $V_{IN_}$ の場合における図1のアナログ-デジタル変換回路1の動作および各部の電圧レンジは、図20のアナログ-デジタル変換回路100と同様である。

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【0085】ここでは、アナログ入力信号の電圧レンジが $V_{IN_}/2$ の場合における図1のアナログ-デジタル変換回路1の動作および各部の出力電圧レンジについて説明する。

【0086】サンプルホールド回路2は、アナログ入力信号 V_{in} をサンプリングして一定時間保持する。サンプルホールド回路2から出力されたアナログ入力信号 V_{in} は、1段目の回路3へ転送される。

【0087】1段目の回路3において、サブA/Dコンバータ9aは電圧レンジ $V_{IN_}/2$ のアナログ入力信号 V_{in} に対してアナログ-デジタル変換を行う。このときのサブA/Dコンバータ9aのフルスケールレンジは、上記のように $V_{IN_}/2$ に切り替えられてい

*る。

【0088】サブA/Dコンバータ9aのA/D変換結果である上位4ビットのデジタル出力($2^3, 2^2, 2^1, 2^0$)は、D/Aコンバータ10へ転送されるとともに、4つのラッチ回路7を介して出力回路8へ転送される。D/Aコンバータ10は、サブA/Dコンバータ9aのA/D変換結果である上位4ビットのデジタル出力をアナログ信号に変換する。

【0089】D/Aコンバータ10のフルスケールレンジは $V_{IN_}$ に固定されているので、D/Aコンバータ10の正規出力電圧レンジは、次式のように表される。

【0090】

$$\begin{aligned} & \left\{ (1 \text{ 段目の分解能} - 1) \times (D/A \text{ コンバータ } 10 \text{ のフルスケールレンジ}) / \right. \\ & \left. (1 \text{ 段目の分解能}) \right\} \\ & = (2^4 - 1) \times (V_{IN_} / 2) / 2^4 \\ & = 15 V_{IN_} / 16 \end{aligned}$$

一方、演算増幅回路11aは、アナログ入力信号 V_{in} をサンプリングして増幅および保持する。上記のように、アナログ入力信号の電圧レンジが $V_{IN_}/2$ の

※場合には利得は2倍に切り替えられるので、演算増幅回路11aの出力電圧レンジは次式のように表される。

【0091】

$$\begin{aligned} & (\text{アナログ入力信号 } V_{in} \text{ の電圧レンジ}) \times (\text{演算増幅回路 } 11a \text{ の利得}) \\ & = (V_{IN_} / 2) \times 2 \\ & = V_{IN_} \end{aligned}$$

減算増幅回路14は、演算増幅回路11aから出力されたアナログ入力信号 V_{in} とD/Aコンバータ10のD/A変換結果とを減算して増幅する。減算増幅回路14★

★の出力は、2段目の回路4へ転送される。

【0092】1段目の減算増幅回路14の出力電圧レンジは、次式のように表される。

$$\begin{aligned} & ((\text{演算増幅回路 } 11a \text{ の出力電圧レンジ}) - (D/A \text{ コンバータ } 10 \text{ の正規} \\ & \text{出力電圧レンジ})) \times (\text{減算増幅回路 } 14 \text{ の利得}) \\ & = ((V_{IN_}) - (15 V_{IN_} / 16)) \times 2 \\ & = V_{IN_} / 8 \end{aligned}$$

2段目の回路4においては、サブA/Dコンバータ9が、1段目の回路3の減算増幅回路14の出力に対してA/D変換を行う。サブA/Dコンバータ9のA/D変換結果は、D/Aコンバータ10へ転送されるとともに、3つのラッチ回路7を介して出力回路8へ転送される。これにより、2段目の回路4から中上位2ビットのデジタル出力($2^3, 2^2$)が得られる。

【0093】一方、演算増幅回路11は、1段目の回路3の減算増幅回路14の出力を増幅する。減算増幅回路14は、演算増幅回路11の出力とD/Aコンバータ10のD/A変換結果とを減算して増幅する。減算増幅回路14の出力は、3段目の回路5へ転送される。

【0094】3段目の回路5においては、2段目の回路4の減算増幅回路14の出力に対して2段目の回路4と同様の動作が行われる。それにより、3段目の回路5から中下位2ビットのデジタル出力($2^3, 2^1$)が得られる。

【0095】4段目の回路6においては、3段目の回路5の減算増幅回路14の出力に対してサブA/Dコンバータ9がA/D変換を行い、下位2ビットのデジタル出

力($2^3, 2^0$)が得られる。

【0096】1段目～4段目の回路3～6のデジタル出力は、各ラッチ回路7を経て同時に出力回路8に到達する。すなわち、各ラッチ回路7は各回路3～6のデジタル出力の同期をとるために設けられている。

【0097】出力回路8は、アナログ入力信号 V_{in} の10ビットのデジタル出力 D_{out} を必要の場合はデジタル補正処理後パラレル出力する。

【0098】上記のように、アナログ入力信号の電圧レンジが $V_{IN_}/2$ の場合には、1段目の回路3の演算増幅回路11aの利得および1段目の回路3のサブA/Dコンバータ9aのフルスケールレンジを切り替えることにより、1段目の回路3の減算増幅回路14から2段目の回路5へ与えられる出力信号の電圧レンジは、アナログ入力信号の電圧レンジが $V_{IN_}$ の場合と同様に、 $V_{IN_}/8$ となる。それにより、アナログ入力信号 V_{in} の電圧レンジが半分になったにもかかわらず、アナログ入力信号の電圧レンジは半分になる前と同じデジタル出力が得られる。

【0099】したがって、回路設計の変更を行うことな

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く、アナログ入力信号の電圧レンジの変更に対応したアナログ-デジタル変換回路を提供することができる。

【0100】本実施の形態によれば、回路構成を変更することなく、差動ダブルエンド入力方式のアナログ-デジタル変換回路をシングルエンド入力方式のアナログ-デジタル変換回路に変更することができる。

【0101】図2(a)、(b)は図1のアナログ-デジタル変換回路1をそれぞれ差動ダブルエンド入力方式およびシングルエンド入力方式に切り替える場合の設定を示す図である。

【0102】図2(a)に示すように、差動ダブルエンド入力時には、演算増幅回路11aの利得を1倍に切り替え、サブA/Dコンバータ9aのフルスケールレンジを $2V_{IN_{max}}$ に切り替える。本例では、差動ダブルエンド入力のアナログ入力信号 V_{in} の正側アナログ入力電圧 $V_{in}(+)$ は1.0Vから2.0Vの範囲で変化し、負側アナログ入力電圧 $V_{in}(-)$ は2.0Vから1.0Vの範囲で変化する。アナログ入力信号 V_{in} の電圧レンジは、次式のようになる。

【0103】 $2V_{IN_{max}} = \{V_{in}(+) - V_{in}(-)\}$ の最大値 - $\{V_{in}(+) - V_{in}(-)\}$ の最小値 = 2.0[V]

この場合、サブA/Dコンバータ9aの正側基準電圧 $V_{ref}(+)$ は1.0Vから2.0Vの範囲で変化し、負側基準電圧 $V_{ref}(-)$ は2.0Vから1.0Vの範囲で変化する。

【0104】図2(b)に示すように、シングルエンド入力時には、演算増幅回路11aの利得を2倍に切り替え、サブA/Dコンバータ9aのフルスケールレンジを $V_{IN_{max}}$ に切り替える。本例では、シングルエンド入力のアナログ入力信号 V_{in} の正側アナログ入力電圧 $V_{in}(+)$ は1.0Vから2.0Vの範囲で変化し、負側アナログ入力電圧 $V_{in}(-)$ は1.5Vで一定である。アナログ入力信号 V_{in} の電圧レンジは、次式のようになる。

【0105】 $V_{IN_{max}} = \{V_{in}(+) - V_{in}(-)\}$ の最大値 - $\{V_{in}(+) - V_{in}(-)\}$ の最小値 = 1.0[V]

この場合、サブA/Dコンバータ9aの正側基準電圧 $V_{ref}(+)$ は1.0Vから2.0Vの範囲で変化し、負側基準電圧 $V_{ref}(-)$ は1.5Vで一定である。

【0106】このように、図1のアナログ-デジタル変換回路1においては、差動ダブルエンド入力方式をシングルエンド入力方式に変更することによりアナログ入力信号の電圧レンジが1/2になっても、回路構成の再設計が不要となる。

【0107】また、シングルエンド入力のアナログ入力信号の電圧レンジを1/2に変更する場合、および差動ダブルエンド入力のアナログ入力信号の電圧レンジを1/2に変更する場合にも、回路構成の再設計が不要とな

る。

【0108】このようにして、同一のLSI(大規模集積回路)において、アナログ入力信号、演算増幅回路の出力、D/A変換回路の出力および演算増幅回路の出力の電圧レンジをプログラマブルに変更することができる。その結果、開発期間の短縮化を図ることができるとともに、低消費電力化を行うことも可能である。

【0109】(2)第2の実施の形態

図3は本発明の第2の実施の形態におけるパイプライン型アナログ-デジタル変換回路の構成を示すブロック図である。図3のアナログ-デジタル変換回路1も、10ビット4段パイプライン構成を有する。

【0110】図3において、アナログ-デジタル変換回路1は、サンプルホールド回路2、1段目～4段目の回路3～6、複数のラッチ回路7および出力回路8から構成されている。

【0111】1段目の回路3は4ビット構成、2～4段目の回路4～6はそれぞれ2ビット構成である。1～3段目の回路3～5において、サブA/Dコンバータ9、9bおよびD/Aコンバータ10、10bのビット数(ビット構成)は同じに設定されている。

【0112】1段目(初段)の回路3は、サブA/Dコンバータ9、D/Aコンバータ10、演算増幅回路11、減算回路12および切り替え可能な利得を有する演算増幅回路13aを備える。減算回路12および演算増幅回路13aが減算増幅回路14aを構成する。

【0113】2段目および3段目の回路4、5は、切り替え可能なフルスケールレンジを有するサブA/Dコンバータ9b、切り替え可能なフルスケールレンジを有するD/Aコンバータ10b、演算増幅回路11、減算回路12および演算増幅回路13を備える。減算回路12および演算増幅回路13が減算増幅回路14を構成する。4段目(最終段)の回路6は、切り替え可能なフルスケールレンジを有するサブA/Dコンバータ9bのみを備える。

【0114】ここでは、2段目～4段目のサブA/Dコンバータ9bが、図20の2段目～4段目のサブA/Dコンバータ9の2倍の精度を有するものとする。以下、2段目～4段目に2倍の精度を有するサブA/Dコンバータ9bを用いた場合のアナログ-デジタル変換回路1の再設計について説明する。

【0115】1段目の回路3内の減算増幅回路14aの利得は1倍と2倍とに切り替え可能である。また、2段目～4段目の回路4～6内のサブA/Dコンバータ9bのフルスケールレンジは $V_{IN_{max}}/8$ と $V_{IN_{max}}/16$ とに切り替え可能である。さらに、2段目および3段目の回路4、5内のD/Aコンバータ10bのフルスケールレンジは $V_{IN_{max}}/4$ と $V_{IN_{max}}/8$ とに切り替え可能である。

【0116】ここでは、1段目の回路3内の減算増幅回

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路14aの利得を1倍に切り替える。また、2段目～4段目の回路4～6内のサブA/Dコンバータ9bのフルスケールレンジを $V_{IN_{max}}/16$ に切り替え、2段目および3段目の回路4、5内のD/Aコンバータ10bのフルスケールレンジを $V_{IN_{max}}/8$ に切り替える。1段目の回路3内のサブA/Dコンバータ9のフルスケールレンジは $V_{IN_{max}}$ である。また、2段目および3段目の回路3、4内の演算増幅回路11、13の利得は2である。

【0117】ここでは、アナログ入力信号の電圧レンジが $V_{IN_{max}}$ の場合における図1のアナログ-デジタル変換回路1の動作および各部の出力電圧レンジについて説明する。

【0118】サンプルホールド回路2は、アナログ入力信号 V_{in} をサンプリングして一定時間保持する。サンプルホールド回路2から出力されたアナログ入力信号 V_{in} は、1段目の回路3へ転送される。

*【0119】1段目の回路3において、サブA/Dコンバータ9は電圧レンジ $V_{IN_{max}}$ のアナログ入力信号 V_{in} に対してアナログ-デジタル変換を行う。このときのサブA/Dコンバータ9のフルスケールレンジは $V_{IN_{max}}$ である。

【0120】サブA/Dコンバータ9のA/D変換結果である上位4ビットのデジタル出力(2^3 、 2^2 、 2^1 、 2^0)は、D/Aコンバータ10へ転送されるとともに、4つのラッチ回路7を介して出力回路8へ転送される。D/Aコンバータ10は、サブA/Dコンバータ9のA/D変換結果である上位4ビットのデジタル出力をアナログ信号に変換する。

【0121】D/Aコンバータ10のフルスケールレンジは固定されているので、D/Aコンバータ10の正規出力電圧レンジは、次式のように表される。

【0122】

$$\begin{aligned} & \text{（1段目の分解能-1）} \times \text{（D/Aコンバータ10のフルスケールレンジ）} / \\ & \text{（1段目の分解能）} \\ & = (2^4 - 1) \times (V_{IN_{max}}) / 2^4 \\ & = 15 V_{IN_{max}} / 16 \end{aligned}$$

一方、演算増幅回路11は、アナログ入力信号 V_{in} をサンプリングして増幅および保持する。演算増幅回路1

※電圧レンジは次式のように表される。

【0123】

1の利得は1倍であるので、演算増幅回路11の出力電

$$\begin{aligned} & \text{（アナログ入力信号} V_{in} \text{の電圧レンジ）} \times \text{（演算増幅回路11の利得）} \\ & = V_{IN_{max}} \times 1 \\ & = V_{IN_{max}} \end{aligned}$$

減算増幅回路14aは、演算増幅回路11から出力されたアナログ入力信号 V_{in} とD/Aコンバータ10のD/A変換結果とを減算して増幅する。減算増幅回路14aの出力は、2段目の回路4へ転送される。

★【0124】1段目の減算増幅回路14aの利得は1に切り替えられているので、1段目の減算増幅回路14aの出力電圧レンジは、次式のように表される。

★【0125】

$$\begin{aligned} & \text{（（演算増幅回路11の出力電圧レンジ）-（D/Aコンバータ10の正規出力電圧レンジ））} \times \text{（減算増幅回路14aの利得）} \\ & = ((V_{IN_{max}}) - (15 V_{IN_{max}} / 16)) \times 1 \\ & = V_{IN_{max}} / 16 \end{aligned}$$

2段目の回路4においては、サブA/Dコンバータ9bが、1段目の回路3の減算増幅回路14aの出力に対してA/D変換を行う。サブA/Dコンバータ9bのA/D変換結果は、D/Aコンバータ10bへ転送されるとともに、3つのラッチ回路7を介して出力回路8へ転送される。

☆

【0127】D/Aコンバータ10bは、サブA/Dコンバータ9bのA/D変換結果である中上位2ビットのデジタル出力をアナログ信号に変換する。

【0126】この場合、サブA/Dコンバータ9bは、図20のサブA/Dコンバータ9の2倍の精度を有するので、図20のサブA/Dコンバータ9の半分のフルスケールレンジ $V_{IN_{max}}/16$ で2段目の回路4から中上位2ビットのデジタル出力(2^1 、 2^0)が得られ

40 【0128】D/Aコンバータ10bのフルスケールレンジは図20のD/Aコンバータ10の半分の $V_{IN_{max}}/8$ に切り替えられているので、D/Aコンバータ10bの正規出力電圧レンジは、次式のように表される。

【0129】

$$\begin{aligned} & \text{（2段目の分解能-1）} \times \text{（D/Aコンバータ10bのフルスケールレンジ）} / \\ & \text{（2段目の分解能）} \\ & = (2^2 - 1) \times (V_{IN_{max}} / 8) / 2^2 \\ & = 3 V_{IN_{max}} / 32 \end{aligned}$$

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$$V_o(-) = (V_{in}(-) - V_{RT1}) \cdot (CA/CB)$$

$$\Delta V_o = V_o(+) - V_o(-)$$

$$= (V_{in}(+) - V_{in}(-)) \cdot (CA/CB)$$

したがって、容量値切り替え回路111、112の容量値CBを切り替えることにより、演算増幅回路11aの利得を切り替えることができる。

【0143】図5は図1のアナログ・デジタル変換回路1における演算増幅回路11aの構成の第2の例を示す回路図である。

【0144】図5の演算増幅回路11aは、演算増幅器110、コンデンサ123、124、容量値切り替え回路125、126およびスイッチ115～122を含む。

【0145】演算増幅器110の反転入力端子と反転出力端子との間にフィードバック容量としてコンデンサ123が接続され、非反転入力端子と非反転出力端子との間にフィードバック容量としてコンデンサ124が接続されている。また、演算増幅器110の反転入力端子に入力容量として容量値切り替え回路125が接続され、非反転入力端子に入力容量として容量値切り替え回路126が接続されている。

$$V_o(+) = (V_{in}(+) - V_{RT1}) \cdot (CC/CD)$$

$$V_o(-) = (V_{in}(-) - V_{RT1}) \cdot (CC/CD)$$

$$\Delta V_o = V_o(+) - V_o(-)$$

$$= (V_{in}(+) - V_{in}(-)) \cdot (CC/CD)$$

したがって、容量値切り替え回路125、126の容量値CCを切り替えることにより、演算増幅回路11aの利得を切り替えることができる。

【0149】図6～図11は演算増幅回路11aの具体的な回路構成の第1～第6の例を示す回路図である。

【0150】図6～図11において、コンデンサCa、Cb、Ccの各々は等しい容量値Cを有するものとする。また、mを任意の正の整数とする。

【0151】図6の例では、演算増幅器110の反転入力端子と反転出力端子との間にm個のコンデンサCaの並列回路とスイッチSaとが直列に接続され、かつm個のコンデンサCaの並列回路が接続されている。ここで、mは任意の正の整数である。同様に、演算増幅器110の非反転入力端子と非反転出力端子との間にm個のコンデンサCaの並列回路とスイッチSaとが直列に接続され、かつm個のコンデンサCaの並列回路が接続されている。また、演算増幅器110の反転入力端子に2m個のコンデンサCbが接続され、非反転入力端子に2m個のコンデンサCbが接続されている。

【0152】正側アナログ入力電圧Vin(+)がそれぞれスイッチS1を介して反転入力端子側の2m個のコンデンサCbに与えられる。また、負側アナログ入力電圧Vin(-)がそれぞれスイッチS1を介して非反転入力端子側のコンデンサCbに与えられる。高電位側基準電圧VRTがそれぞれスイッチS2を介して反転入力端子側のm個のコンデンサCbおよび非反転入力端子側のm個のコンデンサCbに与えられ、低電位側基準電圧VRBがそれぞれスイッチS2を介して非反転入力端子側のm個のコンデンサCbおよび非反転入力端子側のm個のコンデンサCbに与えられる。

*26が接続されている。

【0146】正側アナログ入力電圧Vin(+)および中間基準電圧VRT1がそれぞれスイッチ115、116を介して容量値切り替え回路125に与えられる。また、負側アナログ入力電圧Vin(-)および中間基準電圧VRT1がそれぞれスイッチ117、118を介して容量値切り替え回路126に与えられる。演算増幅器110の反転入力端子、反転出力端子、非反転入力端子および非反転出力端子は、それぞれスイッチ119、120、121、122を介して接地されている。

【0147】ここで、容量値切り替え回路125、126の容量値をそれぞれCCとし、コンデンサ123、124の容量値をそれぞれCDとすると、演算増幅器110の反転出力端子の正側アナログ出力電圧Vo(+)および非反転出力端子の負側アナログ出力電圧Vo(-)は次式のようにになる。

【0148】

$$V_o(+) = (V_{in}(+) - V_{RT1}) \cdot (CC/CD)$$

$$V_o(-) = (V_{in}(-) - V_{RT1}) \cdot (CC/CD)$$

$$\Delta V_o = V_o(+) - V_o(-)$$

$$= (V_{in}(+) - V_{in}(-)) \cdot (CC/CD)$$

のm個のコンデンサCbに与えられ、低電位側基準電圧VRBがそれぞれスイッチS2を介して非反転入力端子側のm個のコンデンサCbおよび非反転入力端子側のm個のコンデンサCbに与えられる。

【0153】本例では、入力容量の値は2mCである。スイッチSaをオンにすると、フィードバック容量の値が2mCとなり、スイッチSaをオフにすると、フィードバック容量の値がmCとなる。したがって、差動ダブルエンド入力時には、スイッチSaをオンに切り替えることにより利得が1倍となり、シングルエンド入力時には、スイッチSaをオフに切り替えることにより利得が2倍となる。

【0154】図7の例では、演算増幅器110の反転入力端子と反転出力端子との間に2m個のコンデンサCaの並列回路と2m個のコンデンサCcの並列回路とが直列に接続され、かつコンデンサCcに並列にスイッチSaが接続されている。同様に、演算増幅器110の非反転入力端子と非反転出力端子との間に2m個のコンデンサCaの並列回路と2m個のコンデンサCcの並列回路とが直列に接続され、かつコンデンサCcに並列にスイッチSaが接続されている。図7の演算増幅回路11aの他の部分の構成は、図6の演算増幅回路11aと同様である。

【0155】本例では、入力容量の値は2mCである。スイッチSaをオンにすると、フィードバック容量の値が2mCとなり、スイッチSaをオフにすると、フィー

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ドバック容量の値が mC となる。したがって、差動ダブルエンド入力時には、スイッチ Sa をオンに切り替えることにより利得が1倍となり、シングルエンド入力時には、スイッチ Sa をオフに切り替えることにより利得が2倍となる。

【0156】図8の例では、演算増幅器110の反転入力端子と反転出力端子との間に $2m$ 個のコンデンサ Ca の並列回路と $2m$ 個のコンデンサ Cc の並列回路とが直列に接続され、かつコンデンサ Ca に並列にスイッチ Sa が接続されている。同様に、演算増幅器110の非反転入力端子と非反転出力端子との間に $2m$ 個のコンデンサ Ca の並列回路と $2m$ 個のコンデンサ Cc の並列回路とが直列に接続され、かつコンデンサ Ca に並列にスイッチ Sa が接続されている。図8の演算増幅回路11aの他の部分の構成は、図6の演算増幅回路11aと同様である。

【0157】本例では、入力容量の値は $2mC$ である。スイッチ Sa をオンにすると、フィードバック容量の値が $2mC$ となり、スイッチ Sa をオフにすると、フィードバック容量の値が mC となる。したがって、差動ダブルエンド入力時には、スイッチ Sa をオンに切り替えることにより利得が1倍となり、シングルエンド入力時には、スイッチ Sa をオフに切り替えることにより利得が2倍となる。

【0158】図9の例では、演算増幅器110の反転入力端子と反転出力端子との間に m 個のコンデンサ Ca の並列回路が接続されている。同様に、演算増幅器110の非反転入力端子と非反転出力端子との間に m 個のコンデンサ Ca の並列回路が接続されている。また、演算増幅器110の反転入力端子に $2m$ 個のコンデンサ Cb が接続され、非反転入力端子に $2m$ 個のコンデンサ Cb が接続されている。

【0159】正側アナログ入力電圧 $V_{in}(+)$ がそれぞれスイッチ $S1$ 、 $S1a$ を介して反転入力端子側の $2m$ 個のコンデンサ Cb に与えられる。また、負側アナログ入力電圧 $V_{in}(-)$ がそれぞれスイッチ $S1$ 、 $S1a$ を介して非反転入力端子側のコンデンサ Cb に与えられる。高電位側基準電圧 V_{RT} がそれぞれスイッチ $S2$ 、 $S2a$ を介して反転入力端子側の m 個のコンデンサ Cb および非反転入力端子側の m 個のコンデンサ Cb に与えられ、低電位側基準電圧 V_{RB} がそれぞれスイッチ $S2$ 、 $S2a$ を介して非反転入力端子側の m 個のコンデンサ Cb および非反転入力端子側の m 個のコンデンサ Cb に与えられる。

【0160】本例では、フィードバック容量の値は mC である。スイッチ $S1a$ 、 $S2a$ をオンにすると、入力容量の値が $2mC$ となり、スイッチ $S1a$ 、 $S2a$ をオフにすると、入力容量の値が mC となる。したがって、差動ダブルエンド入力時には、スイッチ $S1a$ 、 $S2a$ を常にオフにすることにより利得が1倍となり、シング

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ルエンド入力時には、スイッチ $S1a$ 、 $S2a$ をスイッチ $S1$ 、 $S2$ と同様にスイッチング動作することにより利得が2倍となる。

【0161】図10の例では、演算増幅器110の反転入力端子と反転出力端子との間に m 個のコンデンサ Ca の並列回路が接続されている。同様に、演算増幅器110の非反転入力端子と非反転出力端子との間に m 個のコンデンサ Ca の並列回路が接続されている。また、演算増幅器110の反転入力端子に $2m$ 個のコンデンサ Cc の並列回路が接続され、コンデンサ Cc の並列回路に $2m$ 個のコンデンサ Cb が接続され、コンデンサ Cc に並列にスイッチ Sa が接続されている。また、非反転入力端子に $2m$ 個のコンデンサ Cc の並列回路が接続され、コンデンサ Cc の並列回路に $2m$ 個のコンデンサ Cb が接続され、コンデンサ Cc に並列にスイッチ Sa が接続されている。図10の演算増幅回路11aの他の部分の構成は、図6の演算増幅回路11aと同様である。

【0162】本例では、フィードバック容量の値は mC である。スイッチ Sa をオンにすると、入力容量の値が $2mC$ となり、スイッチ Sa をオフにすると、入力容量の値が mC となる。したがって、差動ダブルエンド入力時には、スイッチ Sa をオフにすることにより利得が1倍となり、シングルエンド入力時には、スイッチ Sa をオンにすることにより利得が2倍となる。

【0163】図11の例では、演算増幅器110の反転入力端子と反転出力端子との間に m 個のコンデンサ Ca の並列回路が接続されている。同様に、演算増幅器110の非反転入力端子と非反転出力端子との間に m 個のコンデンサ Ca の並列回路が接続されている。また、演算増幅器110の反転入力端子に $2m$ 個のコンデンサ Cc の並列回路が接続され、コンデンサ Cc の並列回路に $2m$ 個のコンデンサ Cb が接続され、コンデンサ Cb に並列にスイッチ Sa が接続されている。また、非反転入力端子に $2m$ 個のコンデンサ Cc の並列回路が接続され、コンデンサ Cc の並列回路に $2m$ 個のコンデンサ Cb が接続され、コンデンサ Cb に並列にスイッチ Sa が接続されている。図11の演算増幅回路11aの他の部分の構成は、図6の演算増幅回路11aの構成と同様である。

【0164】本例では、フィードバック容量の値は mC である。スイッチ Sa をオンにすると、入力容量の値が $2mC$ となり、スイッチ Sa をオフにすると、入力容量の値が mC となる。したがって、差動ダブルエンド入力時には、スイッチ Sa をオフにすることにより利得が1倍となり、シングルエンド入力時には、スイッチ Sa をオンにすることにより利得が2倍となる。

【0165】図6～図11の演算増幅回路11aにおいて、上記のように、スイッチ Sa はMOSトランジスタにより構成される。それにより、スイッチ Sa が接続されるノードにはMOSトランジスタの並列容量が付加さ

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れ、スイッチS aのオン時にはゲート容量が付加される。演算増幅器110の反転入力端子または非反転入力端子に容量が付加されると、演算増幅回路11aの動作速度が低下する。

【0166】図6および図7の例では、スイッチS aが演算増幅器110の反転出力端子および非反転出力端子に接続されている。それにより、演算増幅回路11aの動作速度が低下しない。したがって、図6および図7の例が好ましい。

【0167】また、スイッチS aがコンデンサに並列に接続された場合、スイッチS aのオン時にオン抵抗が存在するため、コンデンサの容量を完全に切り離すことができない。

【0168】図6の例では、スイッチS aがコンデンサC aに直列に接続されかつスイッチS aが演算増幅器110の反転出力端子および非反転出力端子に接続されている。それにより、スイッチS aのオン時に、コンデンサC aの容量を完全に切り離すことができる。したがって、図6の例が最も好ましい。

【0169】また、図9の例では、スイッチS 1 a、S 2 aがコンデンサC bよりも入力側に接続されている。逆に、コンデンサC bがスイッチS 1 a、S 2 aよりも入力側に接続されている場合、スイッチS 1 a、S 2 aがオフ状態に設定されても、コンデンサC bの寄生容量が充電される。それにより、利得の設定時に、寄生容量を考慮する必要が生じ、寄生容量のばらつきにより利得がばらつくことになる。図9の例のように、スイッチS 1 a、S 2 aがコンデンサC bよりも入力側に接続されることにより、スイッチS 1 a、S 2 aがオフ状態に設定された場合にスイッチS 1 a、S 2 aによりコンデンサC bが寄生容量とともに切り離される。したがって、図9の例では、利得の設定時にコンデンサC bの寄生容量を考慮する必要がなくなり、寄生容量のばらつきによる利得のばらつきがなくなる。

【0170】図12は図1のアナログ-デジタル変換回路1におけるサブA/Dコンバータ9aの構成の第1の例を示す回路図。図13は図12のサブA/Dコンバータ9aに用いられるコンパレータの構成を示す回路図である。

【0171】図12において、サブA/Dコンバータ9aは、基準電圧を発生する基準電圧発生回路92、93a、93bおよび複数のコンパレータ90を備える。

【0172】基準電圧発生回路92は、直列に接続された複数の抵抗Rからなる。基準電圧発生回路93aは、直列に接続された複数の抵抗Rからなる。基準電圧発生回路93bは、直列に接続された複数の抵抗R1からなる。複数の抵抗Rは等しい抵抗値を有し、複数の抵抗R1は等しい抵抗値を有する。

【0173】基準電圧発生回路92は、高電位側基準電圧VRTを受けるノードN91と低電位側基準電圧VR

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Bを受けるノードN92との間に接続されている。基準電圧発生回路93aは、高電位側基準電圧VRTを受けるノードN93と低電位側基準電圧VRBを受けるノードN94との間に、スイッチS24、S25を介して接続されている。基準電圧発生回路93bは、高電位側基準電圧VRTを受けるノードN93と低電位側基準電圧VRBを受けるノードN94との間に接続されている。基準電圧発生回路93aの中間ノードN95と基準電圧発生回路93bの中間ノードN96との間には、スイッチS26が接続されている。

【0174】基準電圧発生回路92の抵抗R間の接続点にそれぞれ異なる基準電圧が生成される。同様に、基準電圧発生回路93aの抵抗R間の接続点にそれぞれ異なる基準電圧が生成される。ここでは、基準電圧発生回路92により得られる異なる基準電圧を正側基準電圧Vref(+)と呼ぶ。基準電圧発生回路93aにより得られる異なる基準電圧を負側基準電圧Vref(-)と呼ぶ。

【0175】基準電圧発生回路93bの中間ノードN96には、高電位側基準電圧VRTと低電位側基準電圧VRBとの中間の電圧である中間基準電圧VRT1(=(VRT+VRB)/2)が生成される。

【0176】図13に示すように、各コンパレータ90は、演算増幅器91、コンデンサC1、C2およびスイッチS13～S18を含む。演算増幅器91の反転入力端子と反転出力端子との間にスイッチS13が接続され、非反転入力端子と非反転出力端子との間にスイッチS14が接続されている。また、演算増幅器91の反転入力端子にはコンデンサC1が接続され、非反転入力端子にはコンデンサC2が接続されている。コンデンサC1にはスイッチS15、S16が接続され、コンデンサC2にはスイッチS17、S18が接続されている。なお、図12では、各コンパレータ90のスイッチS13、S14の図示を省略している。

【0177】正側アナログ入力電圧Vin(+)および正側基準電圧Vref(+)がそれぞれスイッチS15、S16を介してコンデンサC1に与えられる。また、負側アナログ入力電圧Vin(-)および負側基準電圧Vref(-)がそれぞれスイッチS17、S18を介してコンデンサC2に与えられる。

【0178】初期状態では、スイッチS13、S14、S15、S17がオンし、スイッチS16、S18がオフしている。次に、スイッチS13、S14をオフした後、スイッチS15、S17をオフし、スイッチS16、S18をオンする。スイッチS13、S14をオフした時点で、演算増幅器91の反転入力端子および非反転入力端子がフローティング状態となっているので、反転入力端子の電圧が(Vin(+)-Vref(+))遷移し、非反転入力端子の電圧が(Vin(-)-Vref(-))遷移する。結果的に、差動アナログ入力電

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圧 $(V_{in}(+) - V_{in}(-))$ と差動基準電圧 $(V_{ref}(+) - V_{ref}(-))$ とが比較され、比較結果に応じて正側アナログ出力電圧 $V_{out}(+)$ および負側アナログ出力電圧 $V_{out}(-)$ が変化する。

【0179】図12の複数のコンパレータ90の比較結果をエンコーダ950によってエンコードすることにより、デジタルコード D_{code} を得ることができる。

【0180】図12のサブA/Dコンバータ9aにおいて、差動ダブルエンド入力時には、スイッチS24、S25をオンし、スイッチS26をオフする。それにより、各コンパレータ90のコンデンサC2にスイッチS18を介して基準電圧発生回路93aによりそれぞれ異なる負側基準電圧 $V_{ref}(-)$ が与えられる。シングルエンド入力時には、スイッチS24、S25をオフし、スイッチS26をオンにする。それにより、各コンパレータ90のコンデンサC2にスイッチS18を介して基準電圧発生回路93bにより中間基準電圧 V_{RT1} が与えられる。

【0181】このようにして、サブA/Dコンバータ9aにおいて、フルスケールレンジが切り替えられる。

【0182】なお、基準電圧発生回路93bを設けずに、スイッチS26を基準電圧発生回路93aの中間ノードN95と基準電圧発生回路92の中間ノードとの間に接続してもよい。

【0183】図14は図1のアナログ-デジタル変換回路1におけるサブA/Dコンバータ9aの構成の第2の例を示す回路図。図15は図14のサブA/Dコンバータ9aに用いられるコンパレータの構成を示す回路図である。

【0184】図14において、基準電圧発生回路93aの中間ノードN95と基準電圧発生回路93bの中間ノードN96との間には、図12のスイッチS26が接続されていない。

【0185】図15に示すように、各コンパレータ90は、演算増幅器91、コンデンサC1、C2およびスイッチS13～S18を含み、さらにスイッチS21、S22を含む。スイッチS21の一端はコンデンサC1に接続され、スイッチS21の他端は開放されている。スイッチS22の一端はコンデンサC2に接続され、他端は図14の基準電圧発生回路93bの中間ノードN96に接続されている。図15のコンパレータ90の他の部分の構成は、図13のコンパレータ90の構成と同様である。

【0186】基準電圧発生回路93bにより中間基準電圧 V_{RT1} がスイッチS22を介してコンデンサC2に与えられる。

【0187】差動ダブルエンド入力時の図15のコンパレータ90の動作は、図13のコンパレータ90の動作と同様である。このとき、スイッチS21、S22は常時オフしている。シングルエンド入力時には、スイッチ

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S18の代わりにスイッチS22を動作させる。このとき、スイッチS21は常時オフしている。

【0188】図14のサブA/Dコンバータ9aにおいて、差動ダブルエンド入力時には、スイッチS24、S25をオンする。このとき、スイッチS21、S22は常時オフにする。それにより、各コンパレータ90のコンデンサC2にスイッチS18を介して基準電圧発生回路93aによりそれぞれ異なる負側基準電圧 $V_{ref}(-)$ が与えられる。シングルエンド入力時には、スイッチS24、S25をオフし、スイッチS18の代わりにスイッチS22を動作させる。このとき、スイッチS21は常時オフしている。それにより、各コンパレータ90のコンデンサC2にスイッチS22を介して基準電圧発生回路93bにより中間基準電圧 V_{RT1} が与えられる。

【0189】このようにして、サブA/Dコンバータ9aにおいて、フルスケールレンジが切り替えられる。

【0190】なお、各コンパレータ90にスイッチS21を設けなくてもよいが、コンパレータ90の回路構成の対称性を確保するためには、スイッチS21を設けることが好ましい。

【0191】図16は図3のアナログ-デジタル変換回路1における2段目の回路4内のサブA/Dコンバータ9bの回路図である。図16のサブA/Dコンバータ9bは全並列比較（フラッシュ）方式サブA/Dコンバータである。

【0192】サブA/Dコンバータ9bは、基準電圧を発生する基準電圧発生回路94、95および複数のコンパレータ90から構成される。基準電圧発生回路94、95の各々は、抵抗R2、2n個の抵抗Rおよび抵抗R3からなる。抵抗R2、R3はそれぞれ抵抗Rのn倍の抵抗値を有する。抵抗R2、2n個の抵抗Rおよび抵抗R3は、高電位側基準電圧 V_{RT2} を受けるノードN97と低電位側基準電圧 V_{RB2} を受けるノードN98との間に接続されている。抵抗R2の両端にはスイッチS28が接続され、抵抗R3の両端にはスイッチS29が接続されている。

【0193】基準電圧発生回路94の抵抗R間の接続点にそれぞれ異なる基準電圧が生成される。同様に、基準電圧発生回路95の抵抗R間の接続点にそれぞれ異なる基準電圧が生成される。ここでは、基準電圧発生回路94により得られる異なる基準電圧を正側基準電圧 $V_{ref}(+)$ と呼ぶ。基準電圧発生回路95により得られる異なる基準電圧を負側基準電圧 $V_{ref}(-)$ と呼ぶ。

【0194】正側アナログ入力電圧 $V_{in}(+)$ および正側基準電圧 $V_{ref}(+)$ がそれぞれスイッチS15、S16を介して各コンパレータ90のコンデンサC1に与えられる。また、負側アナログ入力電圧 $V_{in}(-)$ および負側基準電圧 $V_{ref}(-)$ がそれぞれスイッチS17、S18を介して各コンパレータ90のコ

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ンデンサC2に与えられる。図16のコンパレータ90の構成および動作は、図13のコンパレータ90の構成および動作と同様である。

【0195】ここで、高電位側基準電圧VRT2と低電位側基準電圧VRB2との差は $V_{IN..}/8$ に設定される。基準電圧発生回路95、96のスイッチS28、S29がオフの場合には、フルスケールレンジは $V_{IN..}/16$ である。また、スイッチS28、S29をオンにすると、フルスケールレンジは $V_{IN..}/8$ となる。このようにして、サブA/Dコンバータ9bでは、フルスケールレンジを1倍と2倍とに切り替えることができる。

【0196】図17は図3のアナログ-デジタル変換回路1における2段目の回路4内のD/Aコンバータ10の回路図である。図17のD/Aコンバータ10は容量アレイ方式D/Aコンバータである。

【0197】D/Aコンバータ10は、基準電圧を発生する基準電圧発生回路96、アレイ状に接続されたそれぞれ複数個の正側のスイッチS51、S52、複数個の負側のスイッチS53、S54、複数個の正側コンデンサC50、および複数個の負側コンデンサC51から構成される。

【0198】基準電圧発生回路96は、抵抗R4、複数個の抵抗Rおよび抵抗R5からなる。抵抗R4、R5は、複数個の抵抗Rの合計の抵抗値の半分の抵抗値を有する。抵抗R4、複数個の抵抗Rおよび抵抗R5は、高電位側基準電圧VRT3を受けるノードN101と低電位側基準電圧VRB3を受けるノードN102との間に直列に接続されている。抵抗R4の両端にはスイッチS30が接続され、抵抗R5の両端にはスイッチS31が接続されている。

【0199】コンデンサC50、C51はすべて同じ容量値を有する。コンデンサC50の一方の端子（以下、出力端子と呼ぶ）N111からは差動正側出力電圧VDA（+）が生成され、コンデンサC51の一方の端子（以下、出力端子と呼ぶ）N112からは差動負側出力電圧VDA（-）が生成される。なお、各コンデンサC50、C51の他方の端子を入力端子と呼ぶ。

【0200】各スイッチS51の一方の端子は抵抗R4と抵抗Rとの間のノードN103に接続され、他方の端子はコンデンサC50の入力端子に接続されている。各スイッチS52の一方の端子は抵抗R5と抵抗Rとの間のノードN104に接続され、他方の端子はコンデンサC50の入力端子に接続されている。各スイッチS53の一方の端子は抵抗R4と抵抗Rとの間のノードN103に接続され、他方の端子はコンデンサC51の入力端子に接続されている。各スイッチS54の一方の端子は抵抗R5と抵抗Rとの間のノードN104に接続され、他方の端子はコンデンサC51の入力端子に接続されている。

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【0201】スイッチS51、S52、S53、S54は、図16のサブA/Dコンバータ9bのコンパレータ90の出力レベルに従ってオンオフ動作する。同じコンパレータ90の出力信号を受ける4個のスイッチS51、S52、S53、S54が4進スイッチを構成する。例えば、1つのコンパレータ90の出力がハイレベルの場合、4進スイッチのスイッチS51、S54がオンし、スイッチS52、S53がオフする。逆に、1つのコンパレータ90の出力がローレベルの場合、4進スイッチのスイッチS51、S54がオフし、スイッチS52、S53がオンする。

【0202】サブA/Dコンバータ9bの複数のコンパレータ90の出力レベルに応じて複数のスイッチS51、S52、S53、S54がオンオフ動作し、出力端子N111、N112に差動正側出力電圧VDA（+）および差動負側出力電圧VDA（-）が得られる。

【0203】ここで、高電位側基準電圧VRT3と低電位側基準電圧VRB3との差は $V_{IN..}/4$ に設定される。基準電圧発生回路96のスイッチS30、S31がオフの場合には、フルスケールレンジは $V_{IN..}/8$ である。スイッチS30、S31をオンにすると、フルスケールレンジは $V_{IN..}/4$ となる。このようにして、D/Aコンバータ10bでは、フルスケールレンジを1倍と2倍とに切り替えることができる。

【0204】図18は図3のアナログ-デジタル変換回路1における演算増幅回路14aの構成の第1の例を示す回路図である。

【0205】図18の演算増幅回路14aは、演算増幅器130、容量値切り替え回路131、132、コンデンサ133、134およびスイッチ135～138を含む。スイッチは、例えばMOS（金属酸化物半導体）トランジスタにより構成される。

【0206】演算増幅器130の反転入力端子と反転出力端子との間にフィードバック容量として容量値切り替え回路131が接続され、非反転入力端子と非反転出力端子との間にフィードバック容量として容量値切り替え回路132が接続されている。また、演算増幅器130の反転入力端子に入力容量としてコンデンサ133が接続され、非反転入力端子に入力容量としてコンデンサ134が接続されている。

【0207】図3の演算増幅回路11から出力される正側アナログ出力電圧Vo（+）およびD/Aコンバータ10bから出力される差動正側出力電圧VDA（+）がそれぞれスイッチ135、136を介してコンデンサ133に与えられる。また、演算増幅回路11から出力される負側アナログ出力電圧Vo（-）およびD/Aコンバータ10bから出力される差動正側出力電圧VDA（-）がそれぞれスイッチ137、138を介してコンデンサ134に与えられる。演算増幅器130の反転入力端子、反転出力端子、非反転入力端子および非反転出力

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力端子は、それぞれスイッチ139、140、141、142を介して接地されている。

【0208】図18の減算増幅回路14aの動作は、図4の演算増幅回路11aの動作と同様である。演算増幅器130の反転出力端子および非反転出力端子からは次段の回路4へ与えられる正側アナログ入力電圧 V_{in} (+) および負側アナログ入力電圧 V_{in} (-) が得られる。

【0209】ここで、容量値切り替え回路131、132の容量値を切り替えることにより、減算増幅回路14aの利得を切り替えることができる。

【0210】図19は図3のアナログ-デジタル変換回路1における減算増幅回路14aの構成の第2の例を示す回路図である。

【0211】図19の減算増幅回路14aは、演算増幅器130、コンデンサ139、140、容量値切り替え回路141、142およびスイッチ135～140を含む。

【0212】演算増幅器130の反転入力端子と反転出力端子との間にフィードバック容量としてコンデンサ139が接続され、非反転入力端子と非反転出力端子との間にフィードバック容量としてコンデンサ140が接続されている。また、演算増幅器130の反転入力端子に入力容量として容量値切り替え回路141が接続され、非反転入力端子に入力容量として容量値切り替え回路142が接続されている。

【0213】図3の演算増幅回路11から出力される正側アナログ出力電圧 V_o (+) およびD/Aコンバータ10bから出力される差動正側出力電圧 V_{DA} (+) がそれぞれスイッチ135、136を介して容量値切り替え回路141に与えられる。また、演算増幅回路11から出力される負側アナログ出力電圧 V_o (-) およびD/Aコンバータ10bから出力される差動正側出力電圧 V_{DA} (-) がそれぞれスイッチ137、138を介して容量値切り替え回路142に与えられる。演算増幅器130の反転入力端子、反転出力端子、非反転入力端子および非反転出力端子は、それぞれスイッチ139、140、141、142を介して接地されている。

【0214】図19の減算増幅回路14aの動作は、図5の演算増幅回路11aの動作と同様である。演算増幅器130の反転出力端子および非反転出力端子からは次段の回路4へ与えられる正側アナログ入力電圧 V_{in} (+) および負側アナログ入力電圧 V_{in} (-) が得られる。

【0215】ここで、容量値切り替え回路141、142の容量値を切り替えることにより、減算増幅回路14aの利得を切り替えることができる。

【0216】上記の実施の形態のスイッチ S_a 、 S_{1a} 、 S_{2a} 、 S_{24} 、 S_{25} 、 S_{26} 、 S_{28} 、 S_{29} 、 S_{30} 、 S_{31} は、例えばMOS（金属酸化物半導

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体）電界効果トランジスタにより形成される。

【0217】上記実施の形態では、切り替え手段の切り替え部としてスイッチ S_a 、 S_{1a} 、 S_{2a} 、 S_{24} 、 S_{25} 、 S_{26} 、 S_{28} 、 S_{29} 、 S_{30} 、 S_{31} を用いている。この場合には、製造時または使用時にスイッチ S_a 、 S_{1a} 、 S_{2a} 、 S_{24} 、 S_{25} 、 S_{26} 、 S_{28} 、 S_{29} 、 S_{30} 、 S_{31} をオンまたはオフに切り替えることができる。切り替え手段の切り替え部はスイッチに限定されない。例えば、切り替え部としてレーザにより遮断可能なヒューズを用いてもよく、切り替え部として最上層金属のパターニング用マスク切り替え部を用いてもよい。

【0218】図20は切り替え部の他の例を示す回路図である。図20の例では、図6の演算増幅回路11aのスイッチ S_a の代わりにヒューズ F_a を用いている。ヒューズ F_a は、例えばポリシリコンからなり、レーザにより遮断可能である。製造時に、ヒューズ F_a をレーザを用いて遮断するか否かにより演算増幅回路11aの利得を切り替えることができる。

【0219】図21および図22は切り替え部のさらに他の例を示す図であり、上部に平面図を示し、下部に断面図を示す。

【0220】容量形成部500において、下層金属 LM_1 、 LM_2 によりコンデンサの電極501、502が形成されている。また、下層金属 LM_1 により電極507、508が形成されている。さらに、最上層金属 UM により、所定間隔で電極512、513が形成されかつ所定間隔で電極514、515が形成されている。電極501はスルーホール503内の金属を介して電極512に接続され、電極502はスルーホール504内の金属を介して電極514に接続されている。また、電極507はスルーホール505内の金属を介して電極512に接続され、電極508はスルーホール506内の金属を介して電極515に接続されている。

【0221】例えば、507は図6の演算増幅器110の反転入力端子に接続され、電極508は図6の演算増幅器110の反転出力端子に接続される。

【0222】電極501、502により容量形成部500が形成され、電極512、513間および電極514、515間によりマスク切り替え部 MSW がそれぞれ形成される。容量形成ブロック500は、例えば図6のコンデンサ C_a に相当する。

【0223】製造時に、マスク切り替え部 MSW 上に配置するマスクのパターンを変更することにより、電極512、513間および電極514、515間を接続状態および遮断状態に切り替えることができる。

【0224】図21に示すように、電極512、513間および電極514、515間に最上層金属 UM により金属層510、511が形成されるようなマスクを用いることにより、電極512、513間および電極51

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4、515間を接続することができる。

【0225】図22に示すように、電極512、513間および電極514、515間に最上層金属UMにより金属層が形成されないようなマスクを用いることにより、電極512、513間および電極514、515間を遮断することができる。

【0226】図21および図22の例では、容量形成部C500の両方の端子にマスク切り替え部をそれぞれ設けることにより、容量形成部C500を演算増幅器から完全に切り離すことができる。

【0227】なお、本発明は、上記実施の形態に限定されず、アナログ-デジタル変換回路の任意の段の回路において、切り替え可能な利得を有する演算増幅回路、切り替え可能な利得を有する減算増幅回路、切り替え可能なフルスケールレンジを有するサブA/Dコンバータおよび切り替え可能なフルスケールレンジを有するD/Aコンバータのうち少なくとも1つを用いてもよい。

【図面の簡単な説明】

【図1】本発明の第1の実施の形態におけるパイプライン型アナログ-デジタル変換回路の構成を示すブロック図である。

【図2】図1のアナログ-デジタル変換回路をそれぞれ差動ダブルエンド入力方式およびシングルエンド入力方式に切り替える場合の設定を示す図である。

【図3】本発明の第2の実施の形態におけるパイプライン型アナログ-デジタル変換回路の構成を示すブロック図である。

【図4】図1のアナログ-デジタル変換回路における演算増幅回路の構成の第1の例を示す回路図である。

【図5】図1のアナログ-デジタル変換回路における演算増幅回路の構成の第2の例を示す回路図である。

【図6】演算増幅回路の具体的な回路構成の第1の例を示す回路図である。

【図7】演算増幅回路の具体的な回路構成の第2の例を示す回路図である。

【図8】演算増幅回路の具体的な回路構成の第3の例を示す回路図である。

【図9】演算増幅回路の具体的な回路構成の第4の例を示す回路図である。

【図10】演算増幅回路の具体的な回路構成の第5の例を示す回路図である。

【図11】演算増幅回路の具体的な回路構成の第6の例を示す回路図である。

【図12】図1のアナログ-デジタル変換回路におけるサブA/Dコンバータの構成の第1の例を示す回路図である。

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【図13】図12のサブA/Dコンバータに用いられるコンパレータの構成を示す回路図である。

【図14】図1のアナログ-デジタル変換回路におけるサブA/Dコンバータの構成の第2の例を示す回路図である。

【図15】図14のサブA/Dコンバータに用いられるコンパレータの構成を示す回路図である。

【図16】図3のアナログ-デジタル変換回路における2段目の回路内のサブA/Dコンバータの回路図である。

【図17】図3のアナログ-デジタル変換回路における2段目の回路内のD/Aコンバータの回路図である。

【図18】図3のアナログ-デジタル変換回路における減算増幅回路の構成の第1の例を示す回路図である。

【図19】図3のアナログ-デジタル変換回路における減算増幅回路の構成の第2の例を示す回路図である。

【図20】切り替え手段の切り替え部の他の例を示す回路図である。

【図21】切り替え手段の切り替え部のさらに他の例を示す平面図および断面図である。

【図22】切り替え手段の切り替え部のさらに他の例を示す平面図および断面図である。

【図23】従来のアナログ-デジタル変換回路を示すブロック図である。

【図24】図23のアナログ-デジタル変換回路の減算増幅回路の構成を示す回路図およびその減算増幅回路の動作を説明するための図である。

【図25】図23のアナログ-デジタル変換回路において用いられるサブA/Dコンバータの構成を示す図である。

【図26】差動ダブルエンド入力およびシングルエンド入力におけるアナログ-デジタル変換を説明するための図である。

【符号の説明】

1 アナログ-デジタル変換回路

3～6 1段目～4段目の回路

9、9a、9b サブA/Dコンバータ

10、10b D/Aコンバータ

11、13、13a 演算増幅回路

12 減算回路

14、14a 減算増幅回路

VRT、VRT2、VRT3 高電位側基準電圧

VRB、VRB2、VRB3 低電位側基準電圧

VRT1 中間基準電圧

Sa、S1a、S1b、S24、S25、S26、S2

6、S28、S29、S30、S31 スイッチ

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4、515間を接続することができる。

【0225】図22に示すように、電極512、513間および電極514、515間に最上層金属UMにより金属層が形成されないようなマスクを用いることにより、電極512、513間および電極514、515間を遮断することができる。

【0226】図21および図22の例では、容量形成部C500の両方の端子にマスク切り替え部をそれぞれ設けることにより、容量形成部C500を演算増幅器から完全に切り離すことができる。

【0227】なお、本発明は、上記実施の形態に限定されず、アナログ-デジタル変換回路の任意の段の回路において、切り替え可能な利得を有する演算増幅回路、切り替え可能な利得を有する減算増幅回路、切り替え可能なフルスケールレンジを有するサブA/Dコンバータおよび切り替え可能なフルスケールレンジを有するD/Aコンバータのうち少なくとも1つを用いてもよい。

【図面の簡単な説明】

【図1】本発明の第1の実施の形態におけるパイプライン型アナログ-デジタル変換回路の構成を示すブロック図である。

【図2】図1のアナログ-デジタル変換回路をそれぞれ差動ダブルエンド入力方式およびシングルエンド入力方式に切り替える場合の設定を示す図である。

【図3】本発明の第2の実施の形態におけるパイプライン型アナログ-デジタル変換回路の構成を示すブロック図である。

【図4】図1のアナログ-デジタル変換回路における演算増幅回路の構成の第1の例を示す回路図である。

【図5】図1のアナログ-デジタル変換回路における演算増幅回路の構成の第2の例を示す回路図である。

【図6】演算増幅回路の具体的な回路構成の第1の例を示す回路図である。

【図7】演算増幅回路の具体的な回路構成の第2の例を示す回路図である。

【図8】演算増幅回路の具体的な回路構成の第3の例を示す回路図である。

【図9】演算増幅回路の具体的な回路構成の第4の例を示す回路図である。

【図10】演算増幅回路の具体的な回路構成の第5の例を示す回路図である。

【図11】演算増幅回路の具体的な回路構成の第6の例を示す回路図である。

【図12】図1のアナログ-デジタル変換回路におけるサブA/Dコンバータの構成の第1の例を示す回路図である。

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【図13】図12のサブA/Dコンバータに用いられるコンパレータの構成を示す回路図である。

【図14】図1のアナログ-デジタル変換回路におけるサブA/Dコンバータの構成の第2の例を示す回路図である。

【図15】図14のサブA/Dコンバータに用いられるコンパレータの構成を示す回路図である。

【図16】図3のアナログ-デジタル変換回路における2段目の回路内のサブA/Dコンバータの回路図である。

【図17】図3のアナログ-デジタル変換回路における2段目の回路内のD/Aコンバータの回路図である。

【図18】図3のアナログ-デジタル変換回路における減算増幅回路の構成の第1の例を示す回路図である。

【図19】図3のアナログ-デジタル変換回路における減算増幅回路の構成の第2の例を示す回路図である。

【図20】切り替え手段の切り替え部の他の例を示す回路図である。

【図21】切り替え手段の切り替え部のさらに他の例を示す平面図および断面図である。

【図22】切り替え手段の切り替え部のさらに他の例を示す平面図および断面図である。

【図23】従来のアナログ-デジタル変換回路を示すブロック図である。

【図24】図23のアナログ-デジタル変換回路の減算増幅回路の構成を示す回路図およびその減算増幅回路の動作を説明するための図である。

【図25】図23のアナログ-デジタル変換回路において用いられるサブA/Dコンバータの構成を示す図である。

【図26】差動ダブルエンド入力およびシングルエンド入力におけるアナログ-デジタル変換を説明するための図である。

【符号の説明】

1 アナログ-デジタル変換回路

3～6 1段目～4段目の回路

9、9a、9b サブA/Dコンバータ

10、10b D/Aコンバータ

11、13、13a 演算増幅回路

12 減算回路

14、14a 減算増幅回路

VRT、VRT2、VRT3 高電位側基準電圧

VRB、VRB2、VRB3 低電位側基準電圧

VRT1 中間基準電圧

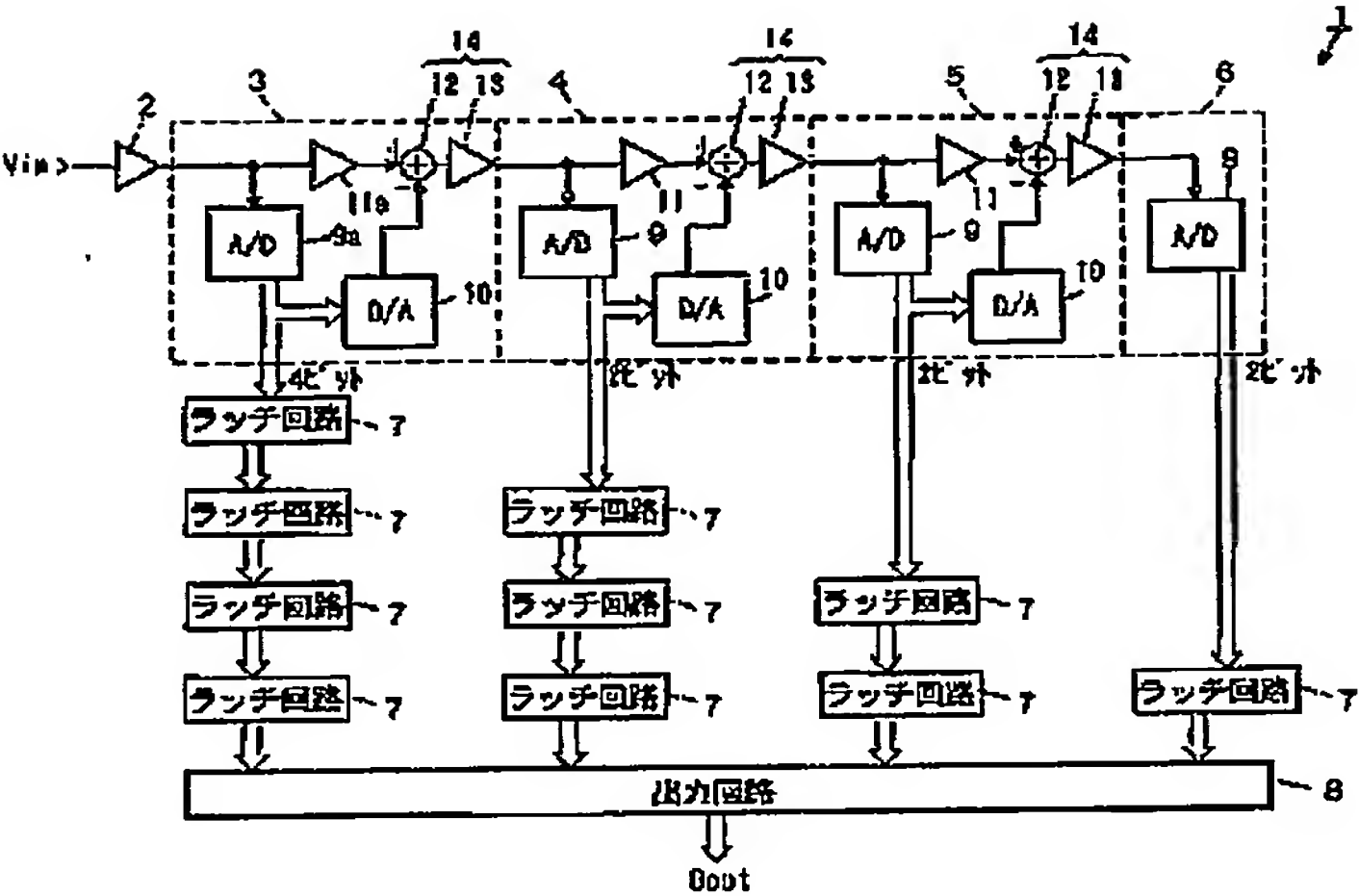
Sa、S1a、S1b、S24、S25、S26、S2

6、S28、S29、S30、S31 スイッチ

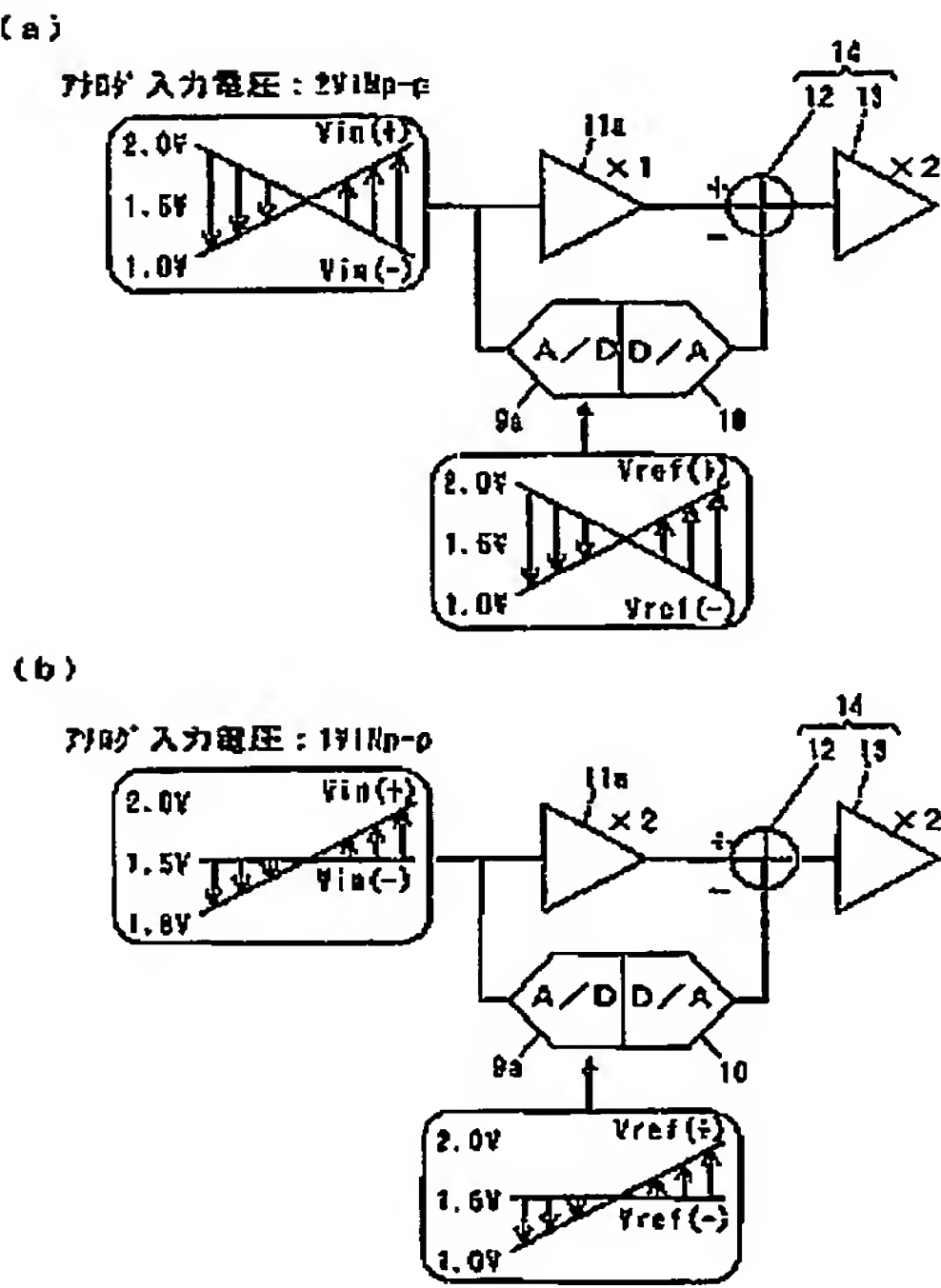
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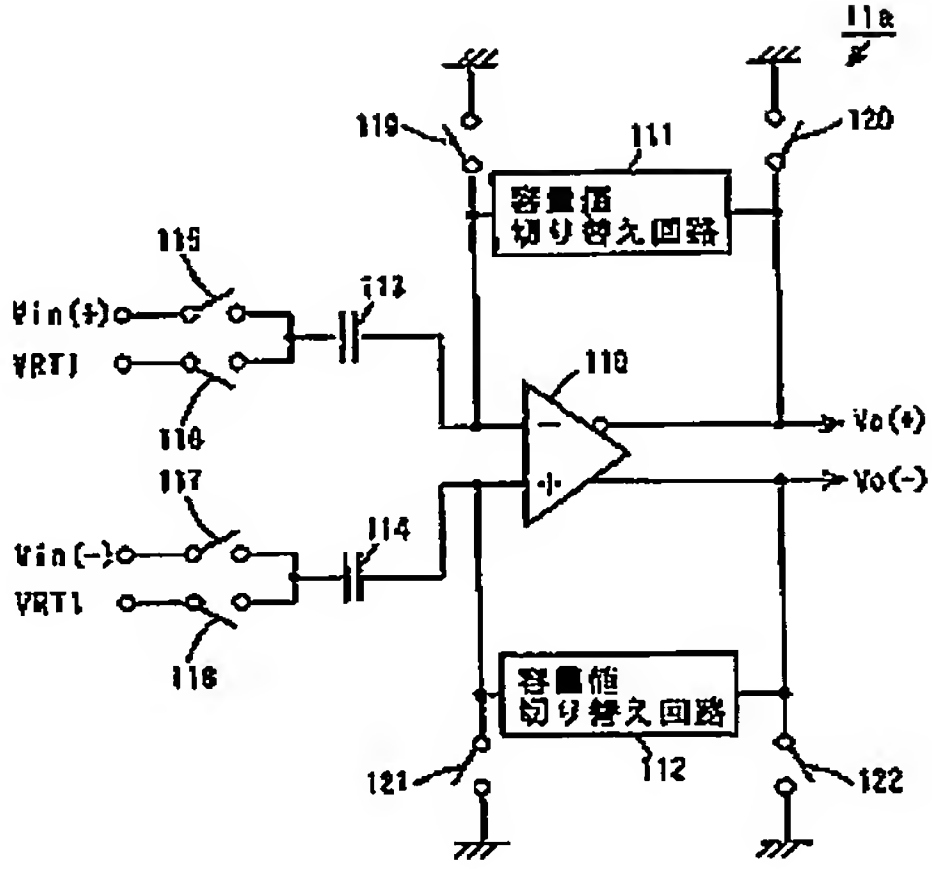
【図1】



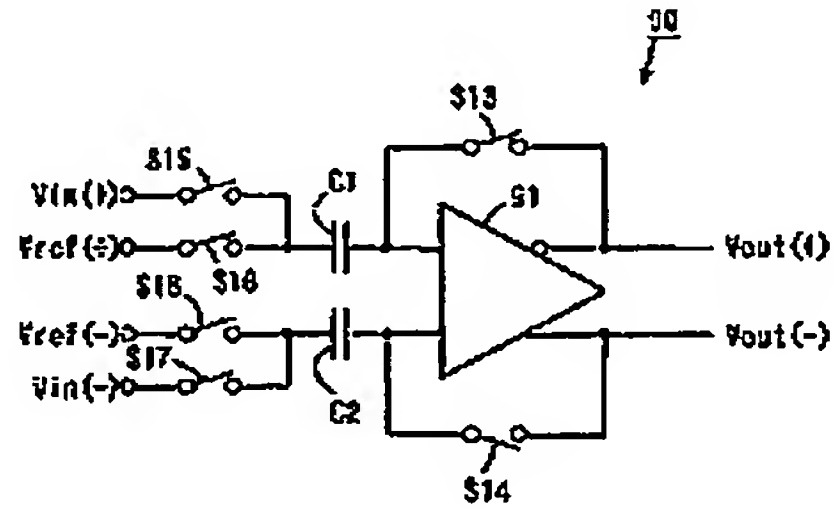
【図2】



【図4】



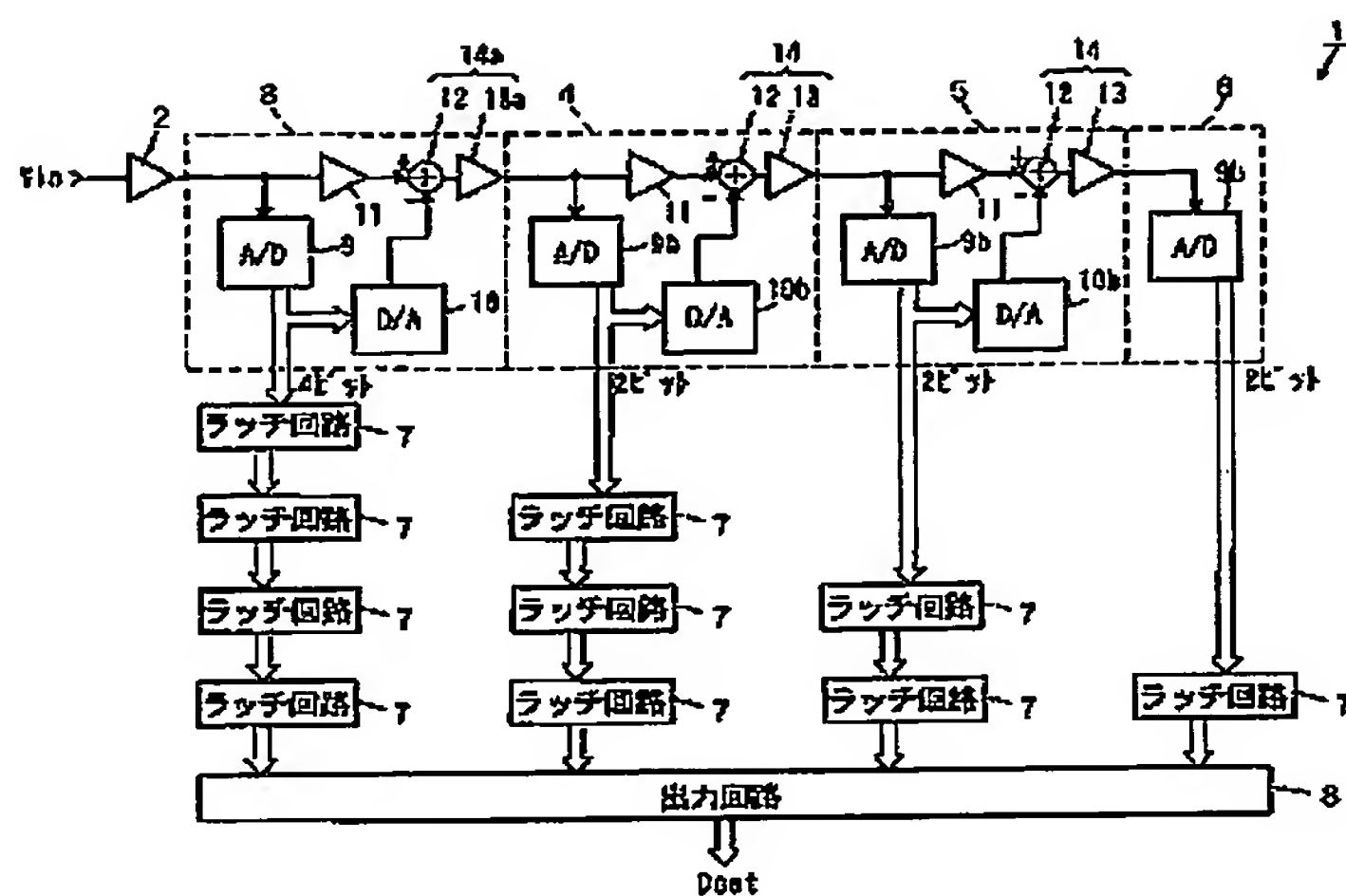
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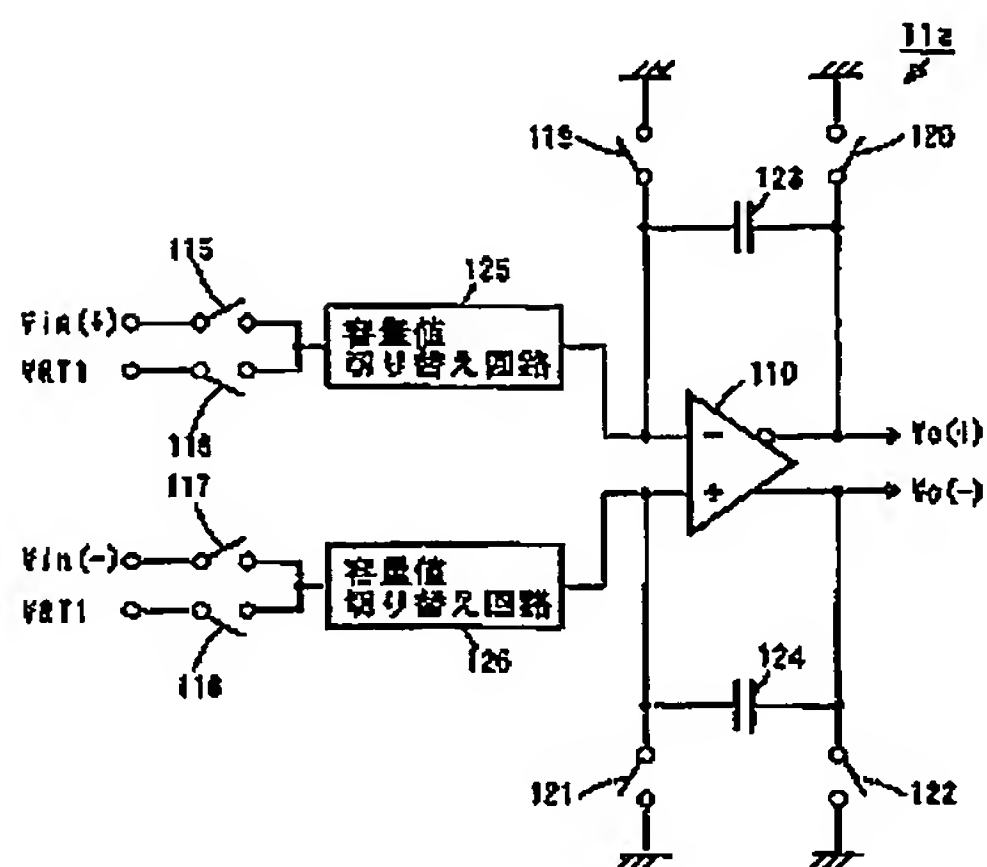
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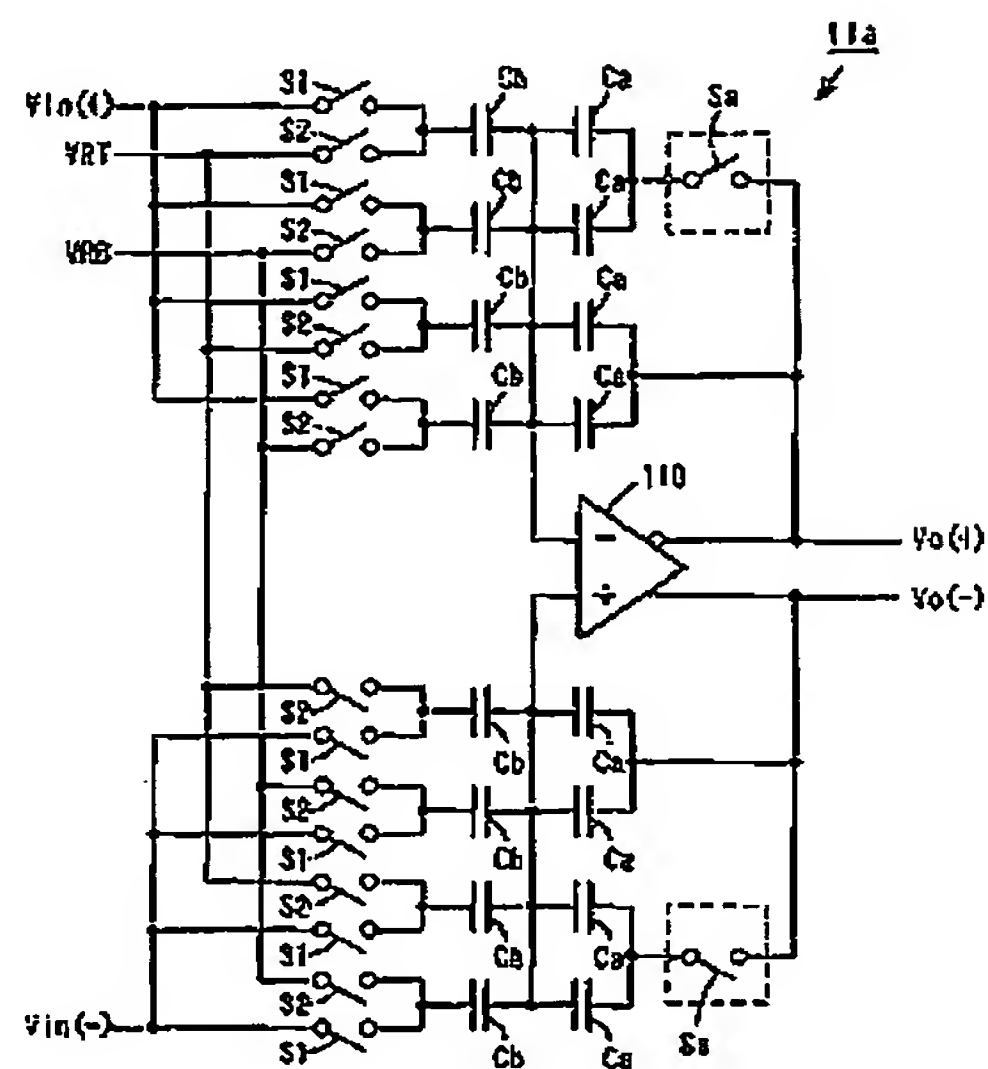
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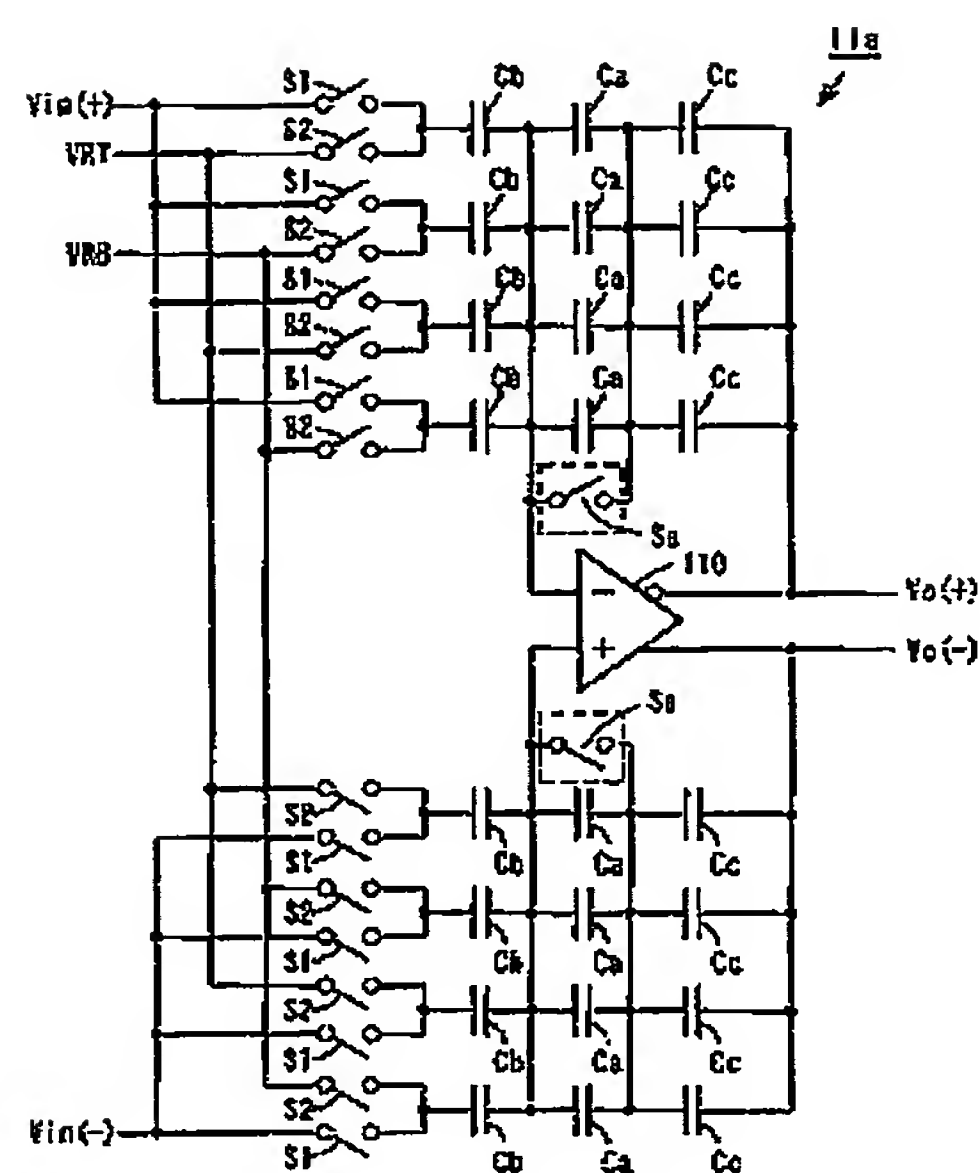
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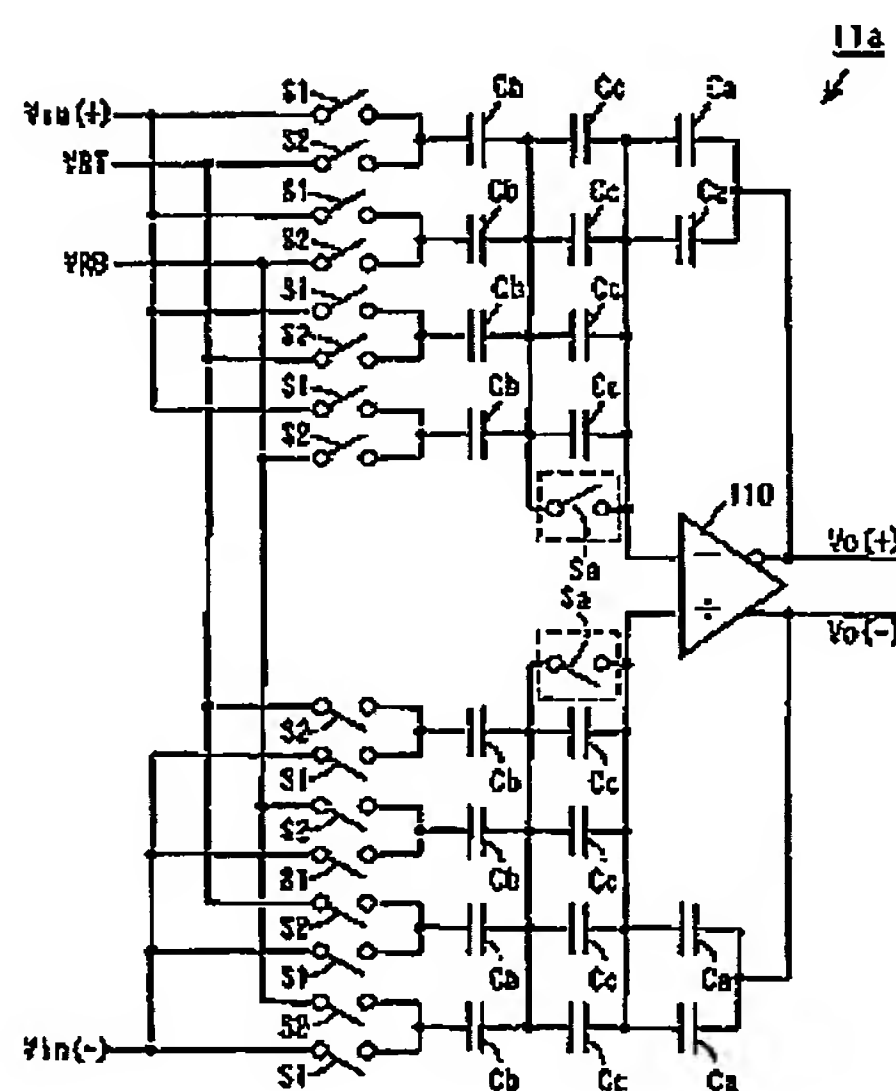
【図6】



【図8】



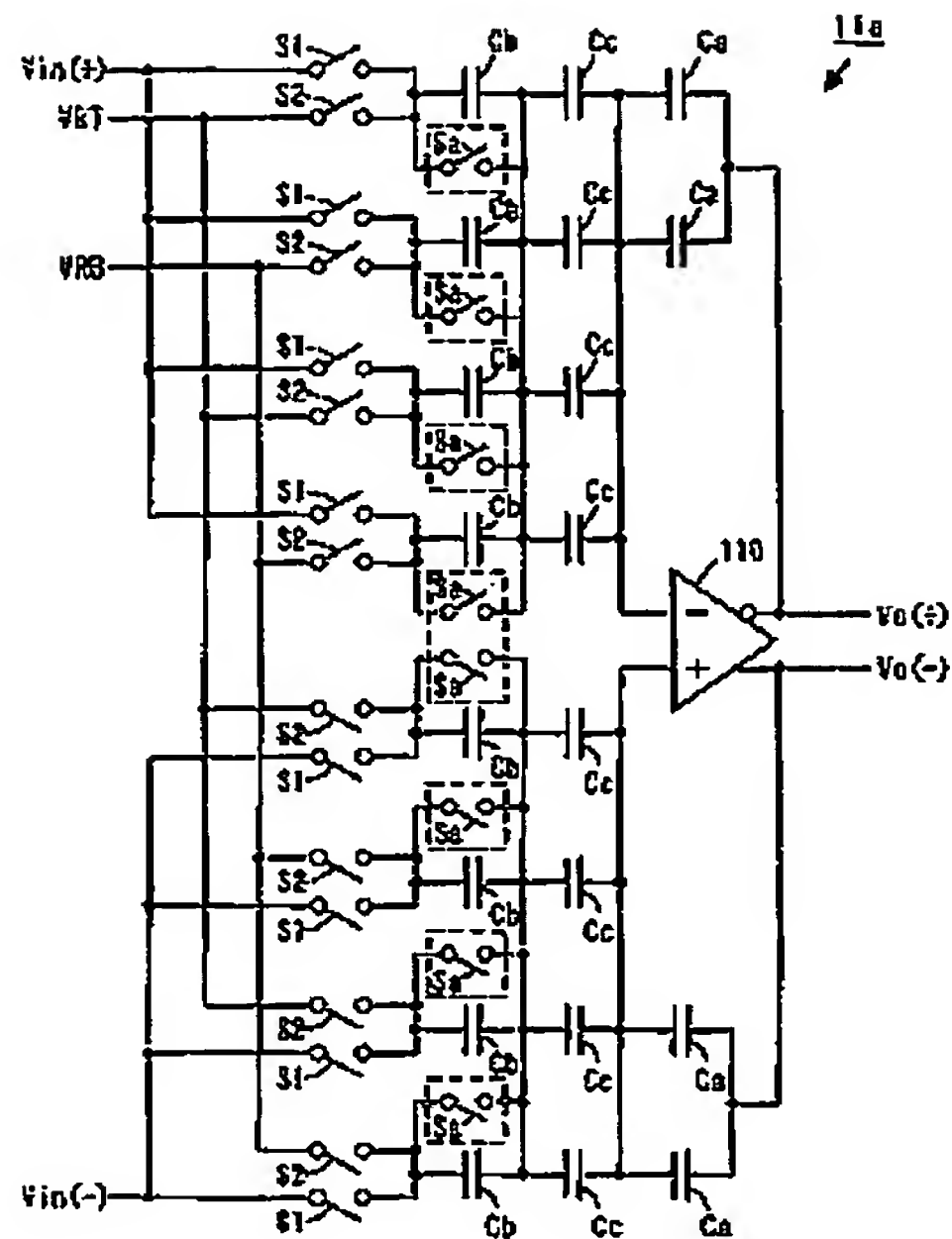
【圖 10】



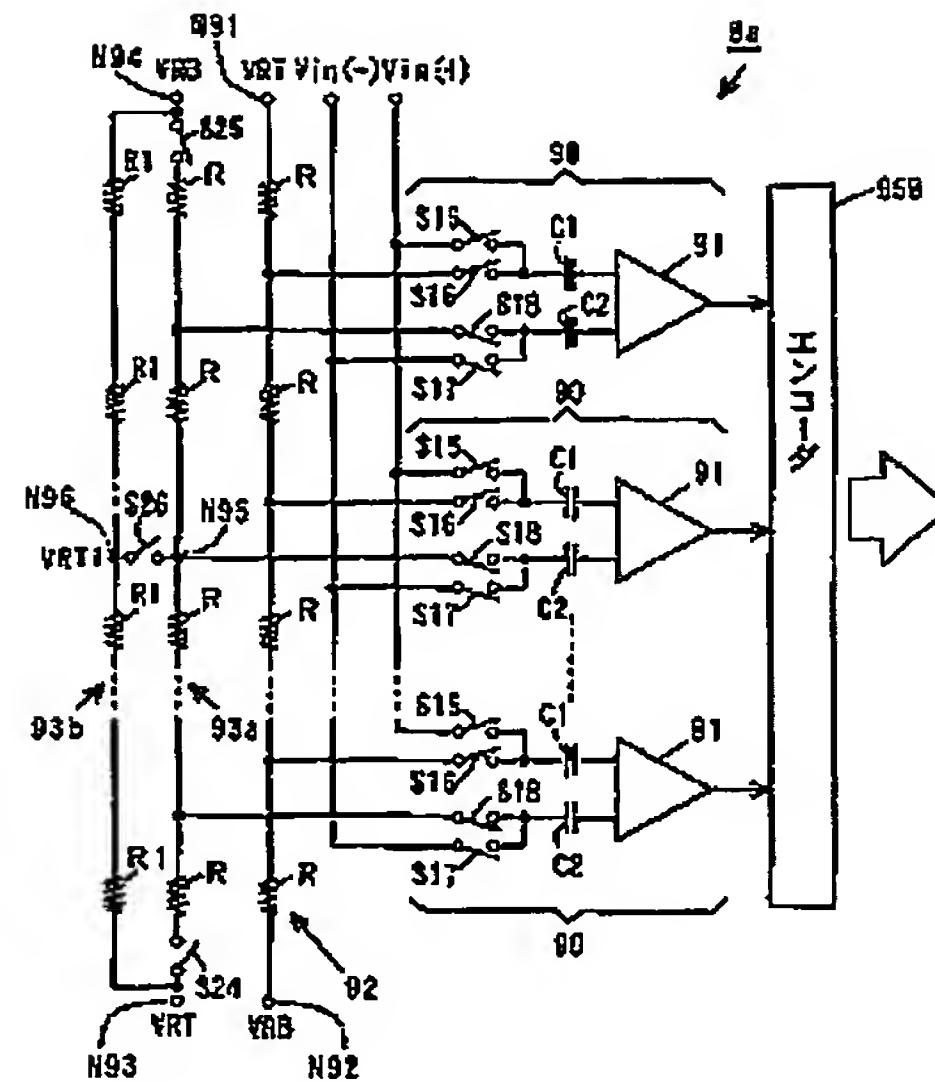
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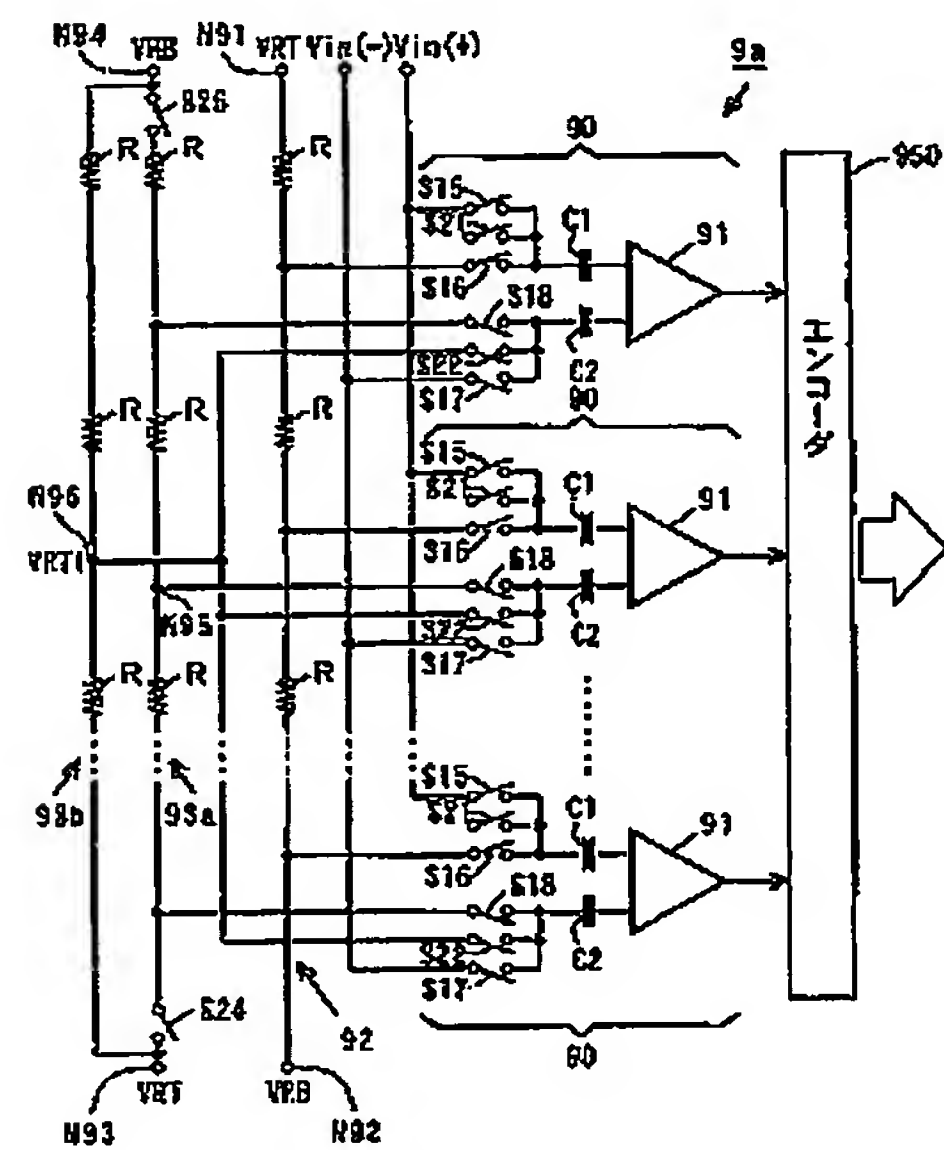
【図11】



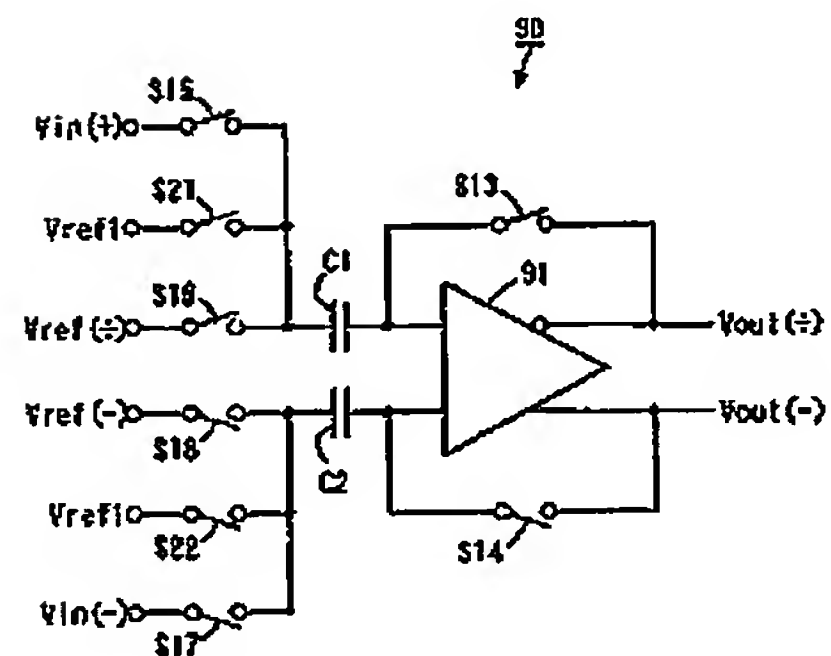
【図12】



【図14】



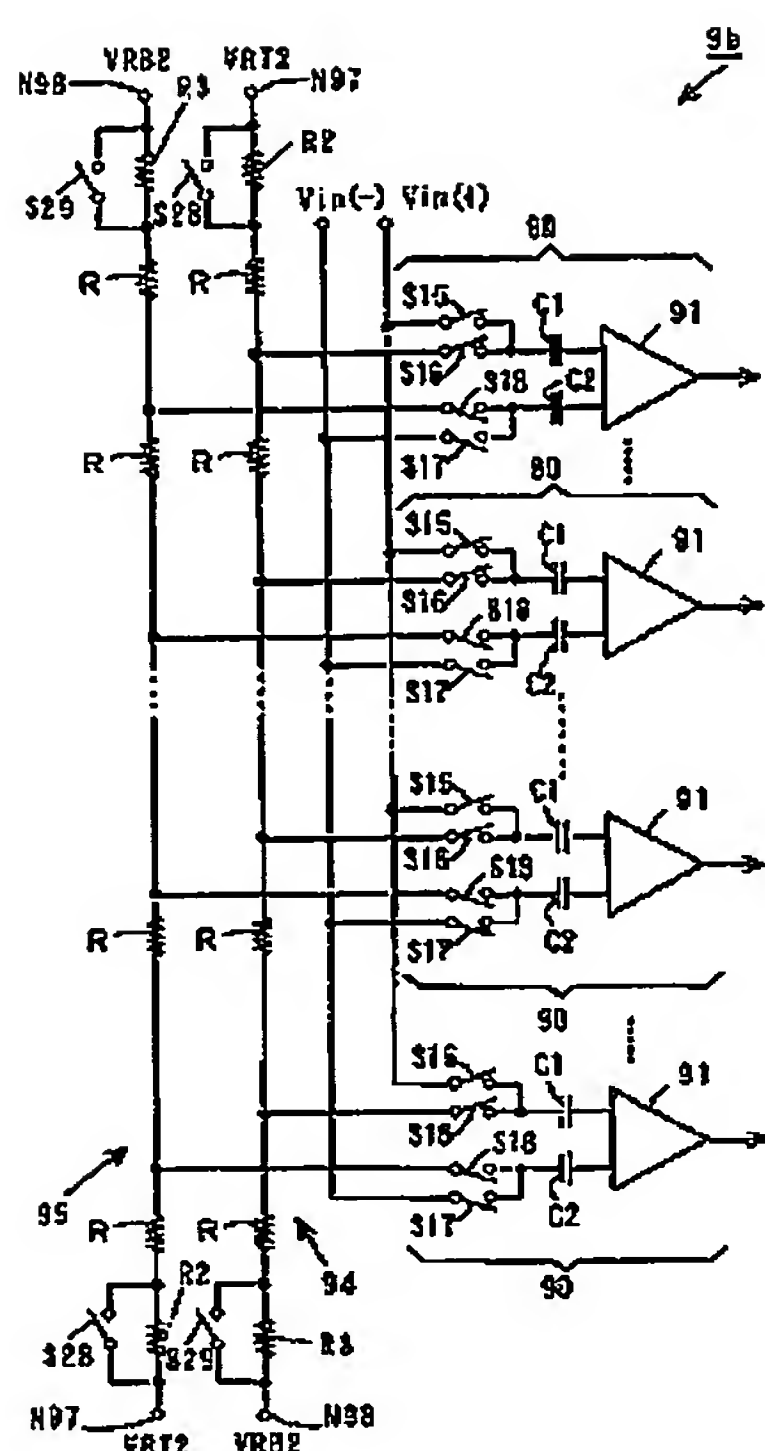
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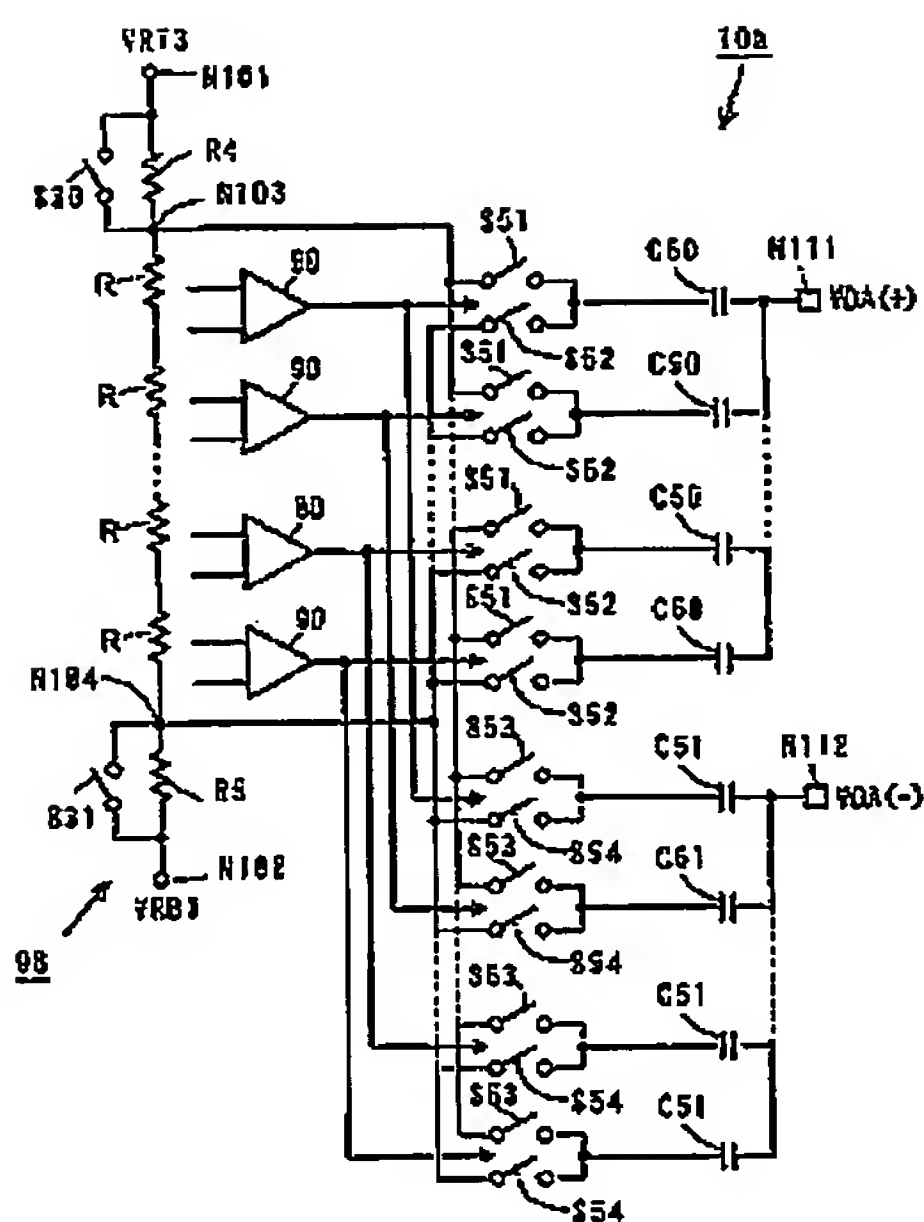
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【圖 16】

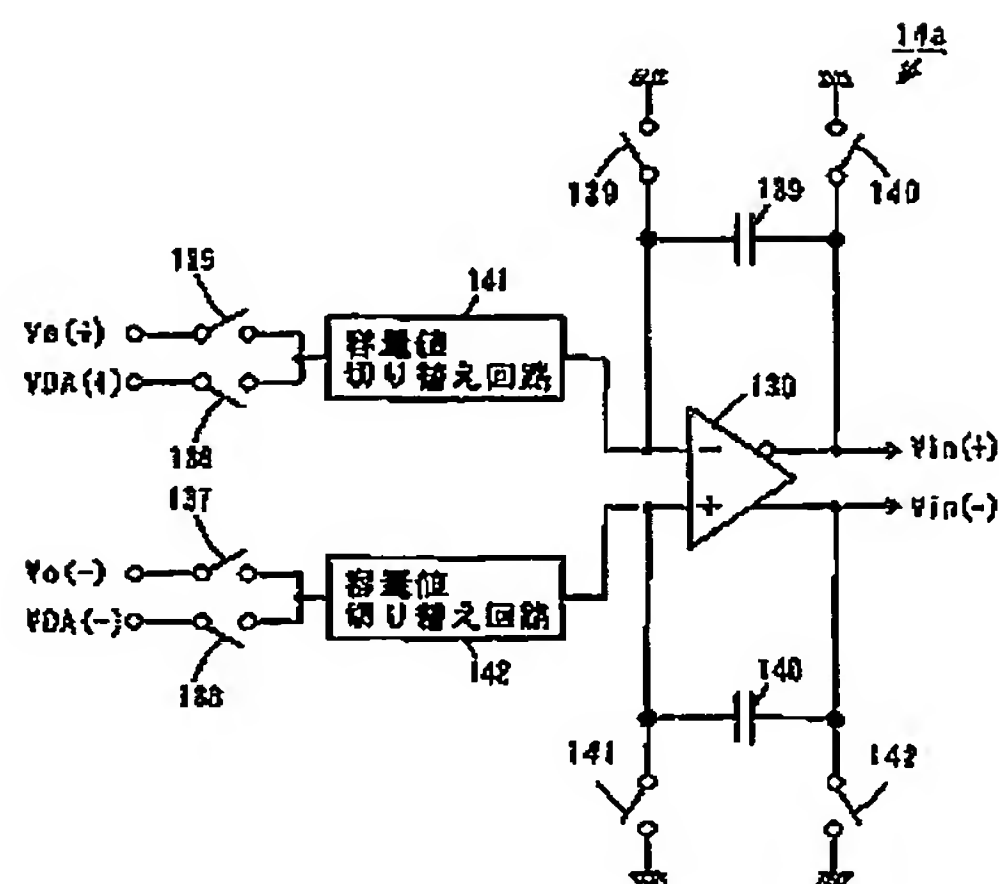
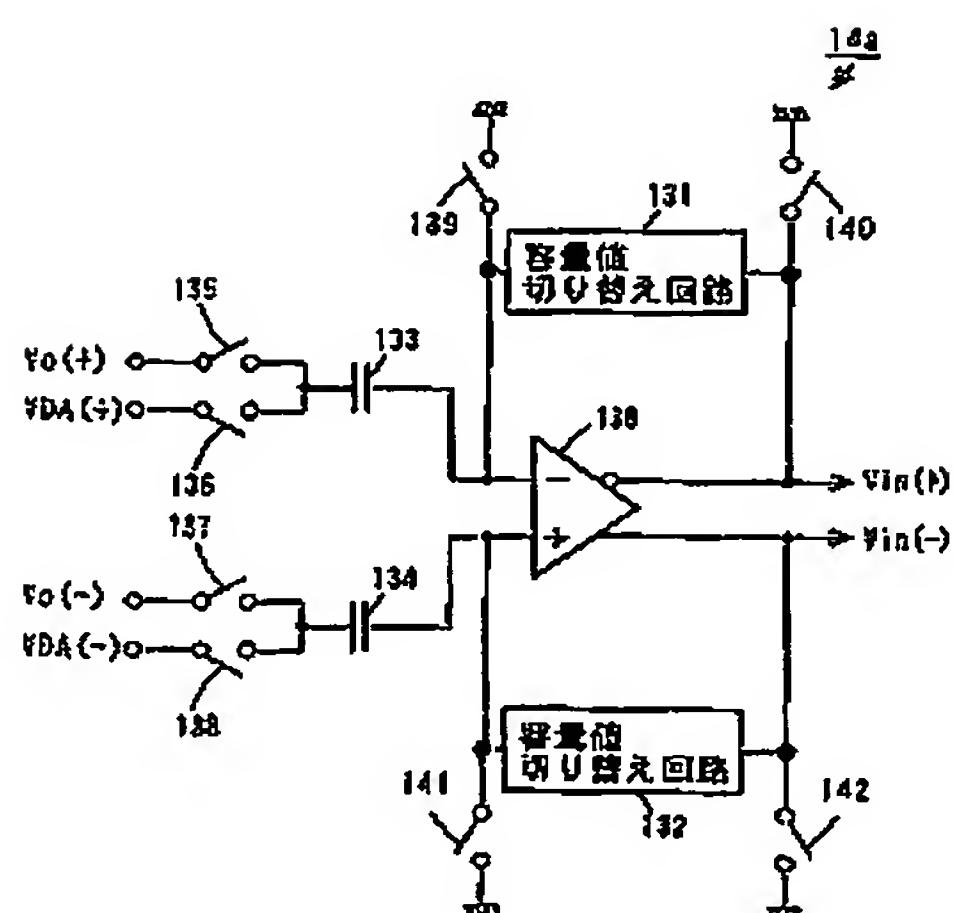


【圖 17】



【圖 19】

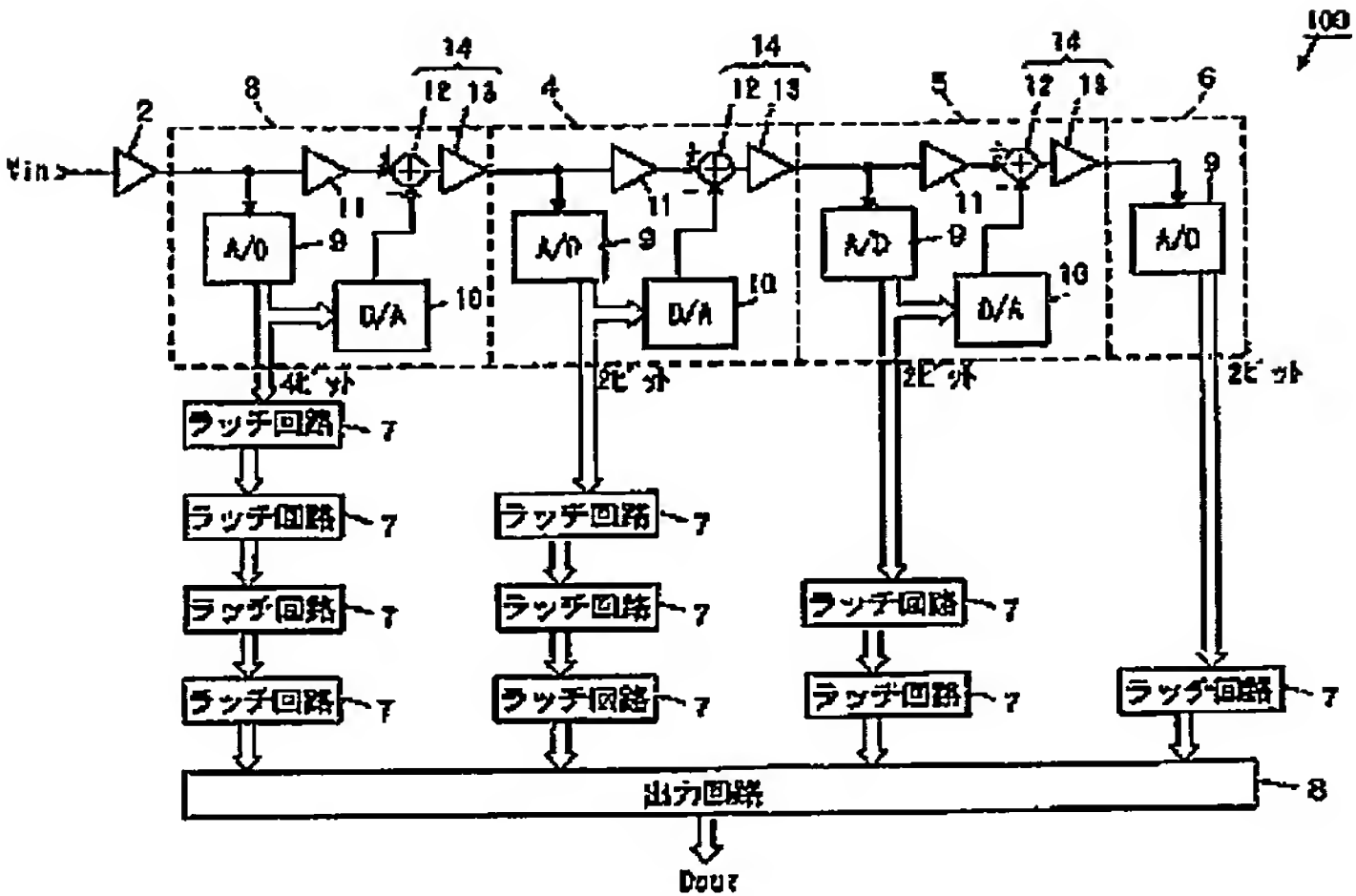
【圖 18】



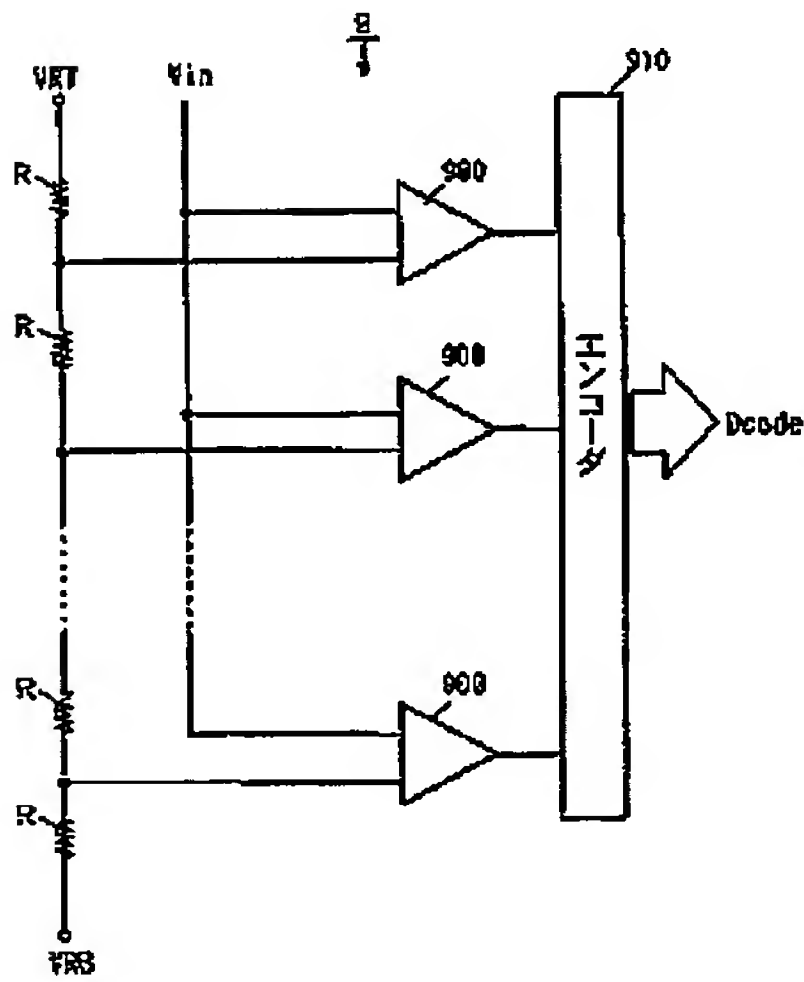
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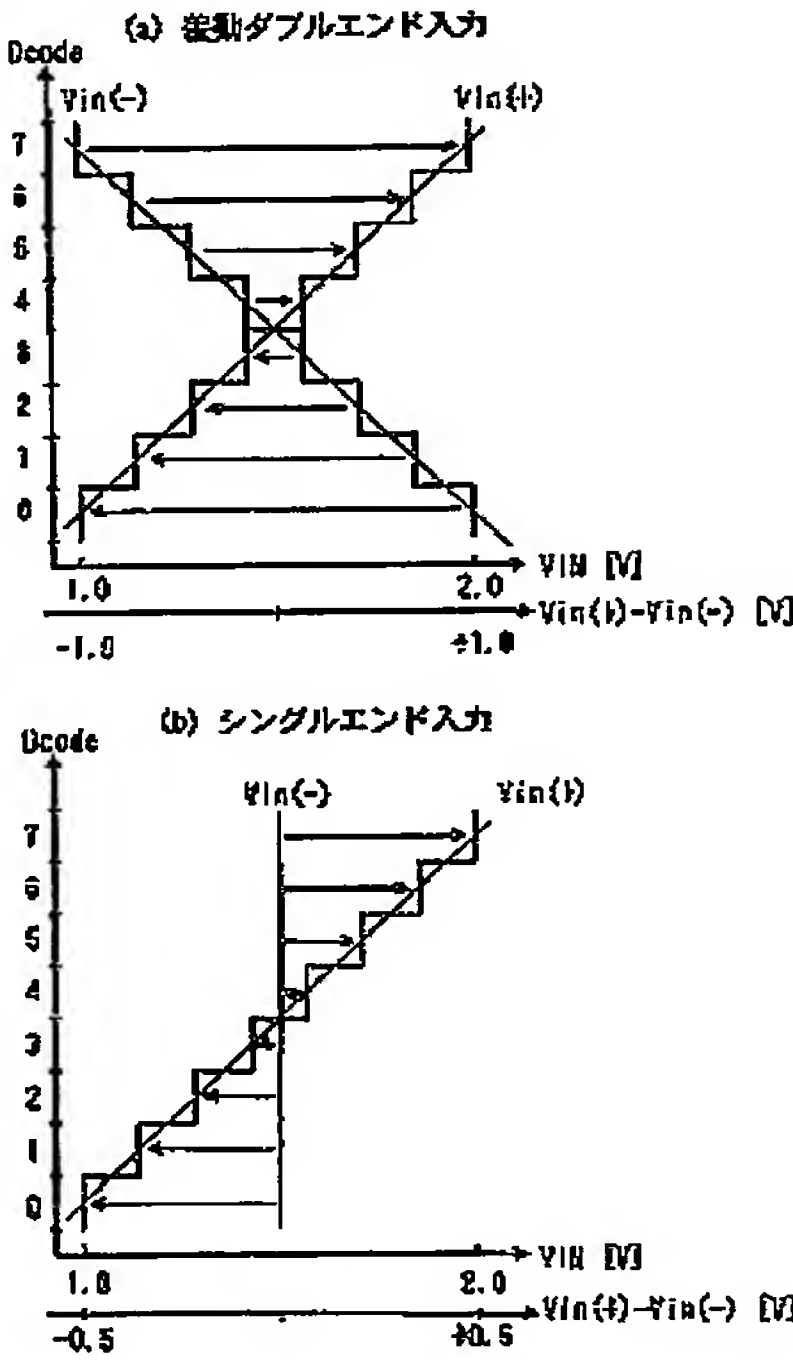
【図23】



【図25】



【図26】



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